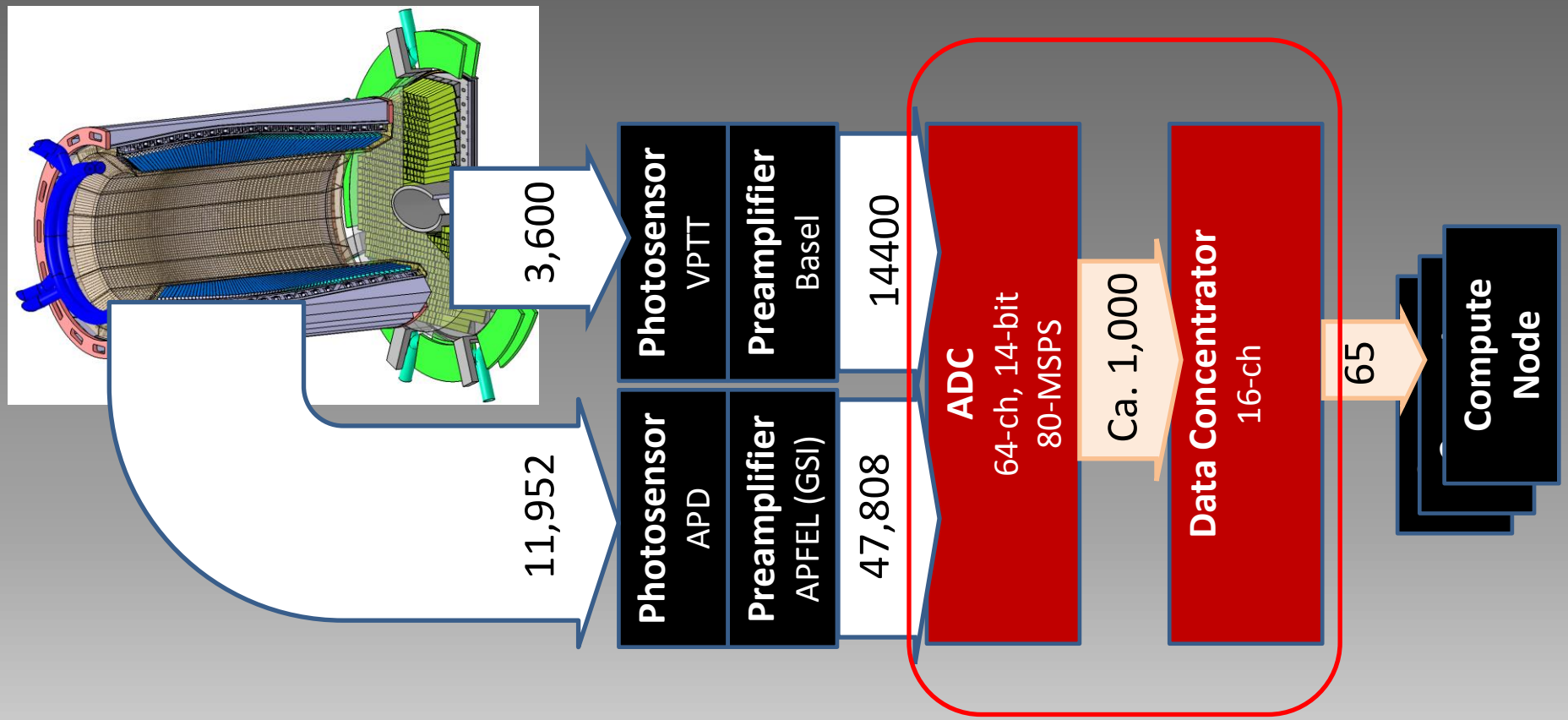
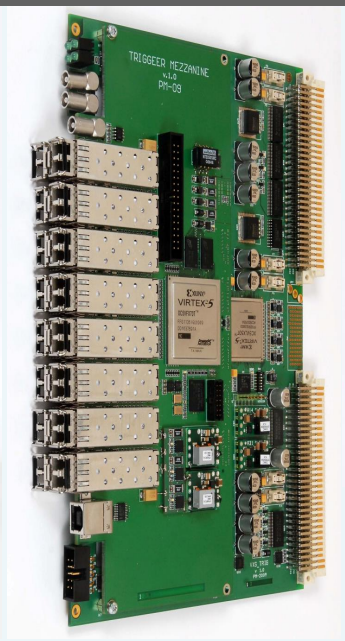
ADC for EMC

- PANDA EMC Readout System



ADC for EMC

- SADC development for PANDA



2008
16-ch, 12-bit
160 MSPS ADC
Used for the first tests, sold to WIENER

2010
16-ch, 2GBit/s
Optical Data Concentrator
Used in many experiments including WASA, KLOE2

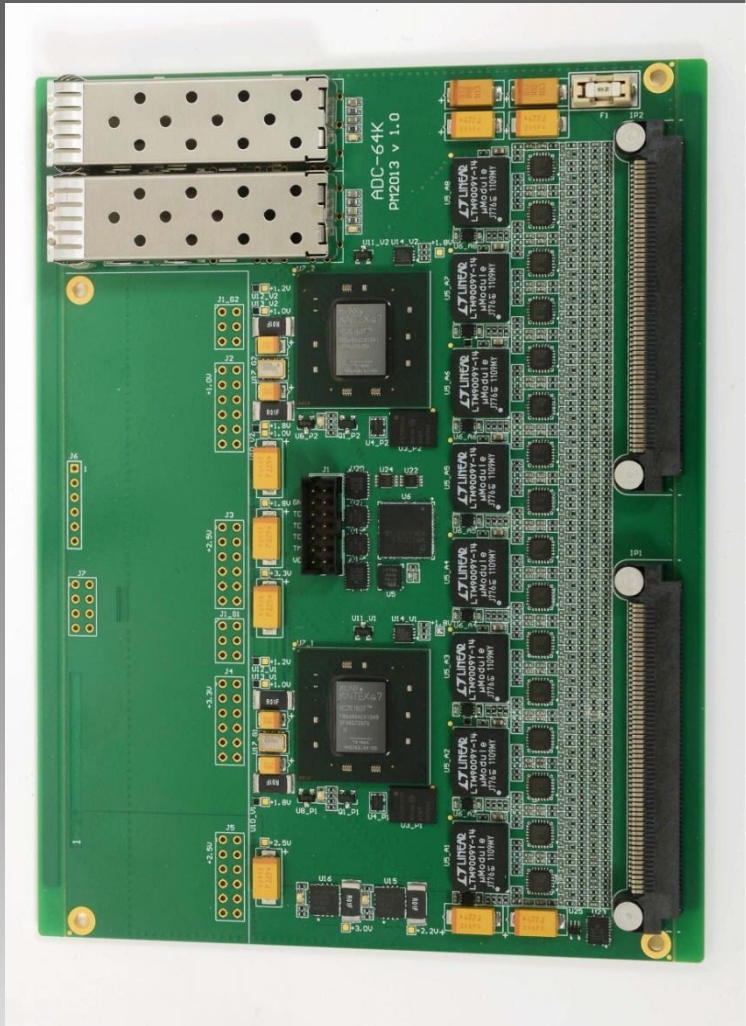
2011
16-ch, 14-bit
125 MSPS ADC
Virtex-5
Used for evaluation of DSP algorithms

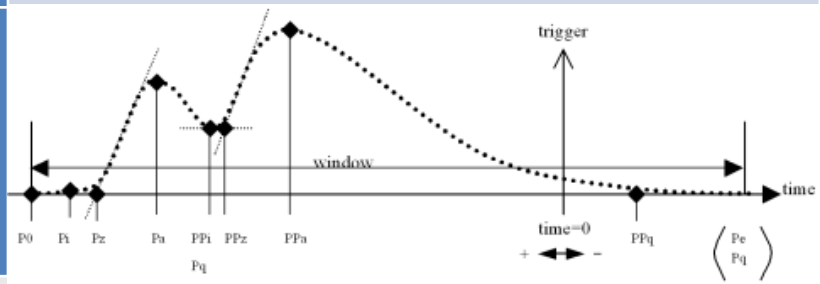
2012
32-ch, Dual-range, 14-bit
80 MSPS ADC
Virtex-6
Used for first data taking and durability tests

2013
64-ch, 14-bit
80 MSPS ADC
Kintex-7
Close-to-final prototype

ADC for EMC

- ADC_64K, a close-to-final prototype



ADC Model	ADC_32DR	ADC_64V	ADC_64K
No. of channels	32 (64)	64	64
Sampling rate	80-125 MSPS		
Input coupling	DC, positive, negative, diff		
Resolution (ampl)	14-bit dual range	14-bit	
Input Connector	uFL	Samtec	
Baseline	0V		
Input range (dual)	±1.0V, ±60 mV	±1.0V, ±100 mV	
Noise	100uV		
Data retention/ch.	25us		
Input filter	Active-filter/Amplifier	CR-passive	Active filter/Amplifier
Interface	Optical, SFP, LC-type, 2 Gbit/s		
Feature extraction:			

ADC for EMC-Endcap

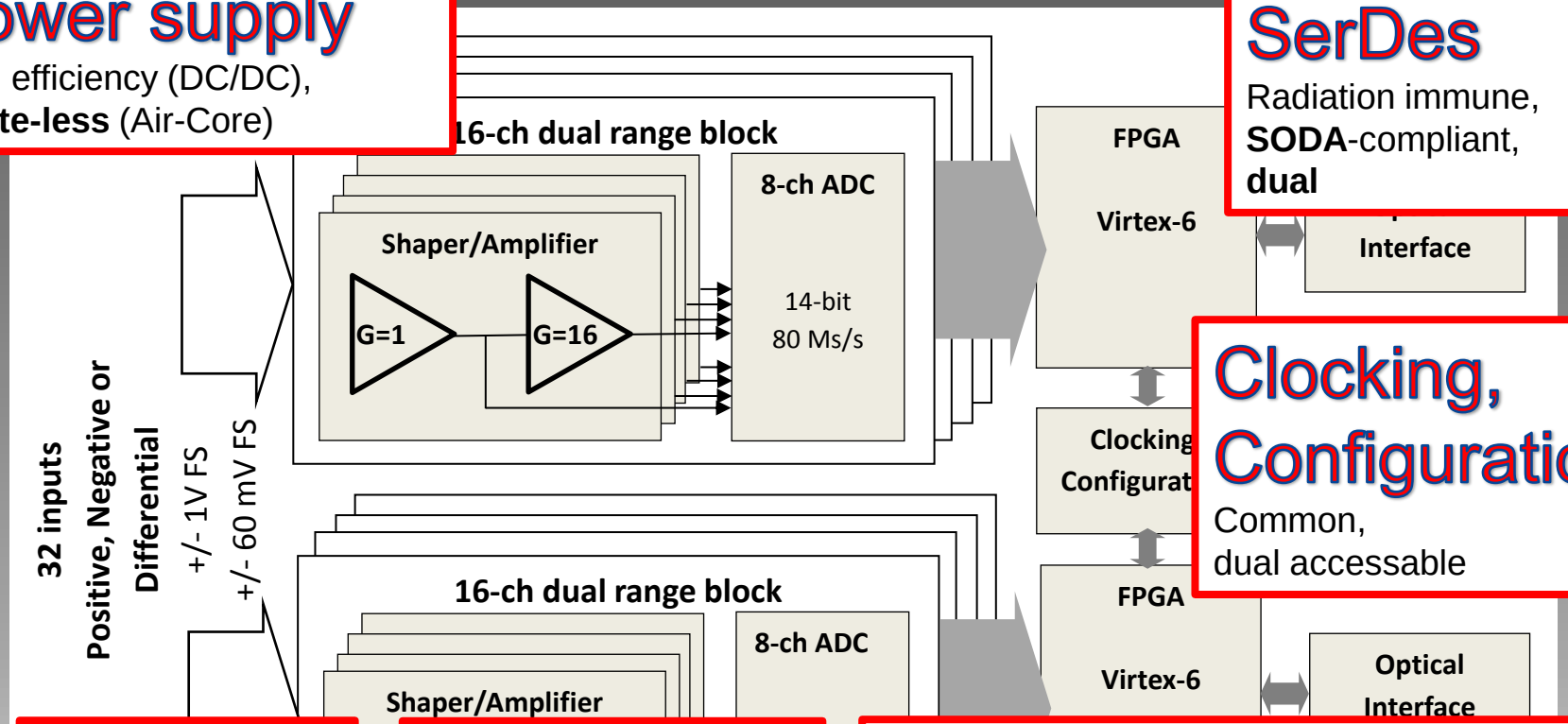
– Design Idea

Power supply

High efficiency (DC/DC),
ferrite-less (Air-Core)

SerDes

Radiation immune,
SODA-compliant,
dual



Clocking, Configuration

Common,
dual accessable

Amplifier

Fully differential,
BW > 100 MHz,
SR > 100 V/us,
Pd < 50 mW/ch,
Active filter

ADC

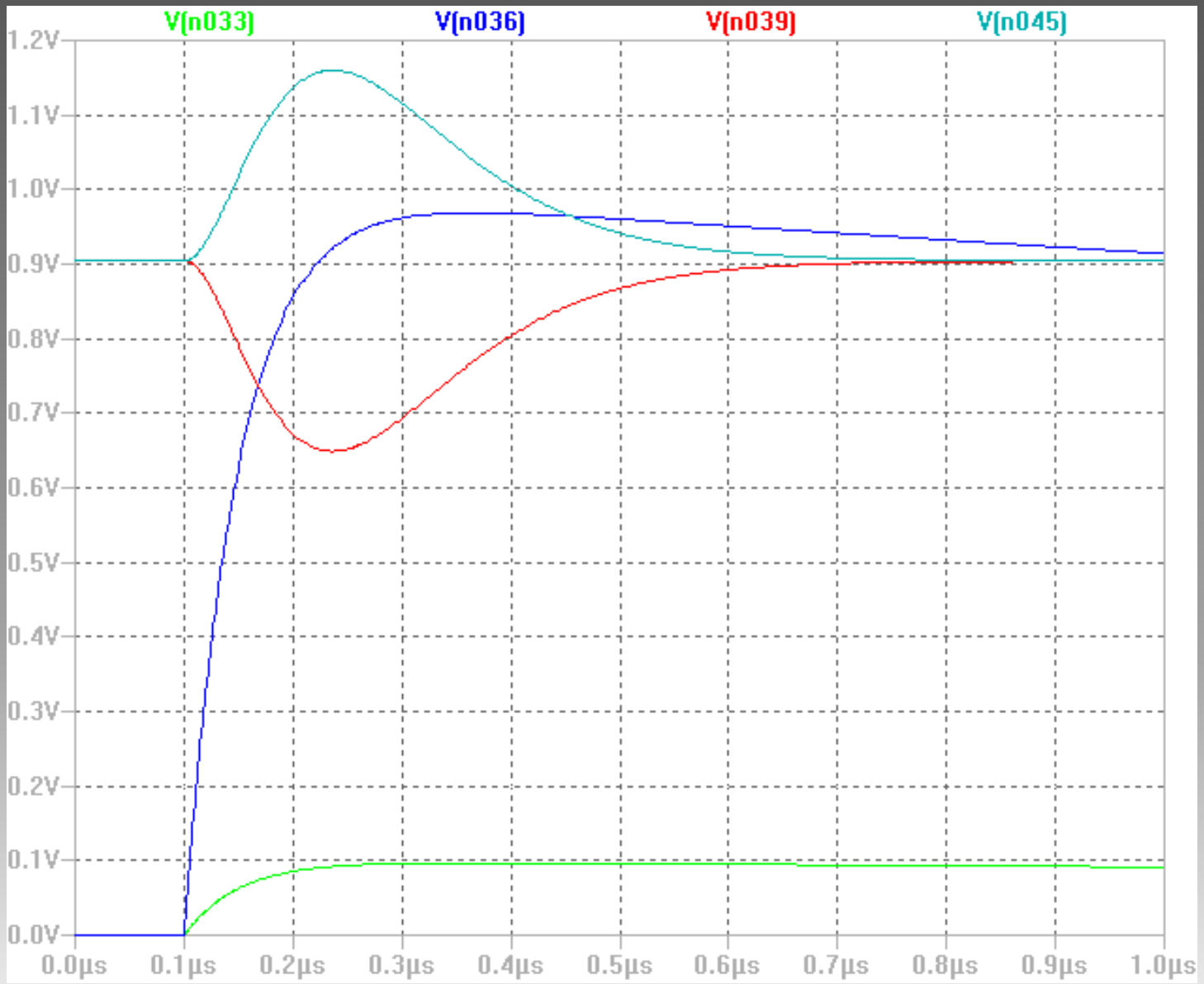
EOB > **14–bit**,
Sampling rate ~**80Ms/s**,
Pd < 100 mW/ch,
32 (64) ch. per board

FPGA

Radiation immune
(RT-Flash or Tripple Modular Redundancy)
or partially reconfigurable with watchdog,
32/64 channels per board

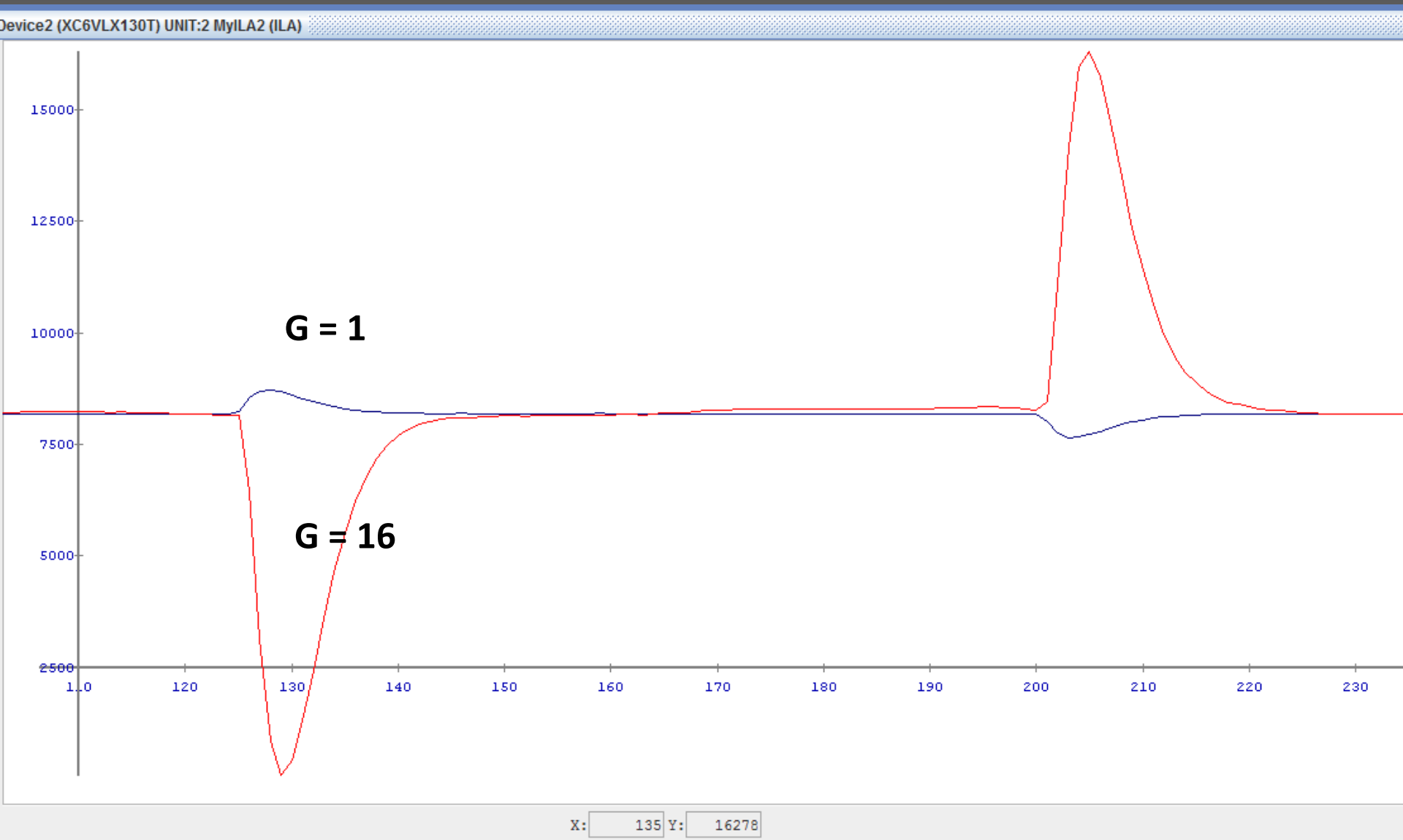
ADC for EMC-Endcap

- Four-pole semi-gaussian shaping



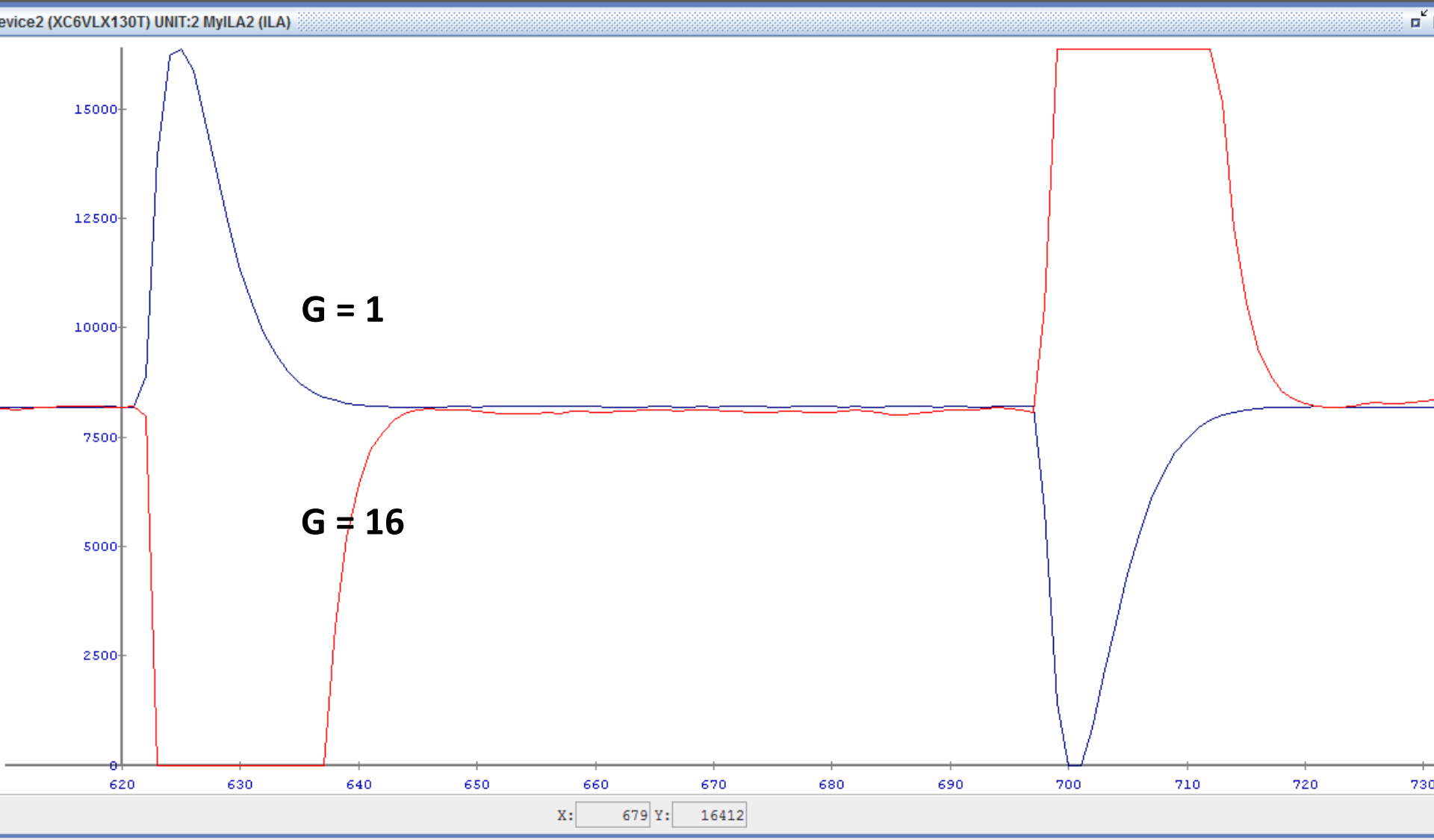
ADC for EMC-Endcap

- 60 mV pulse - bipolar



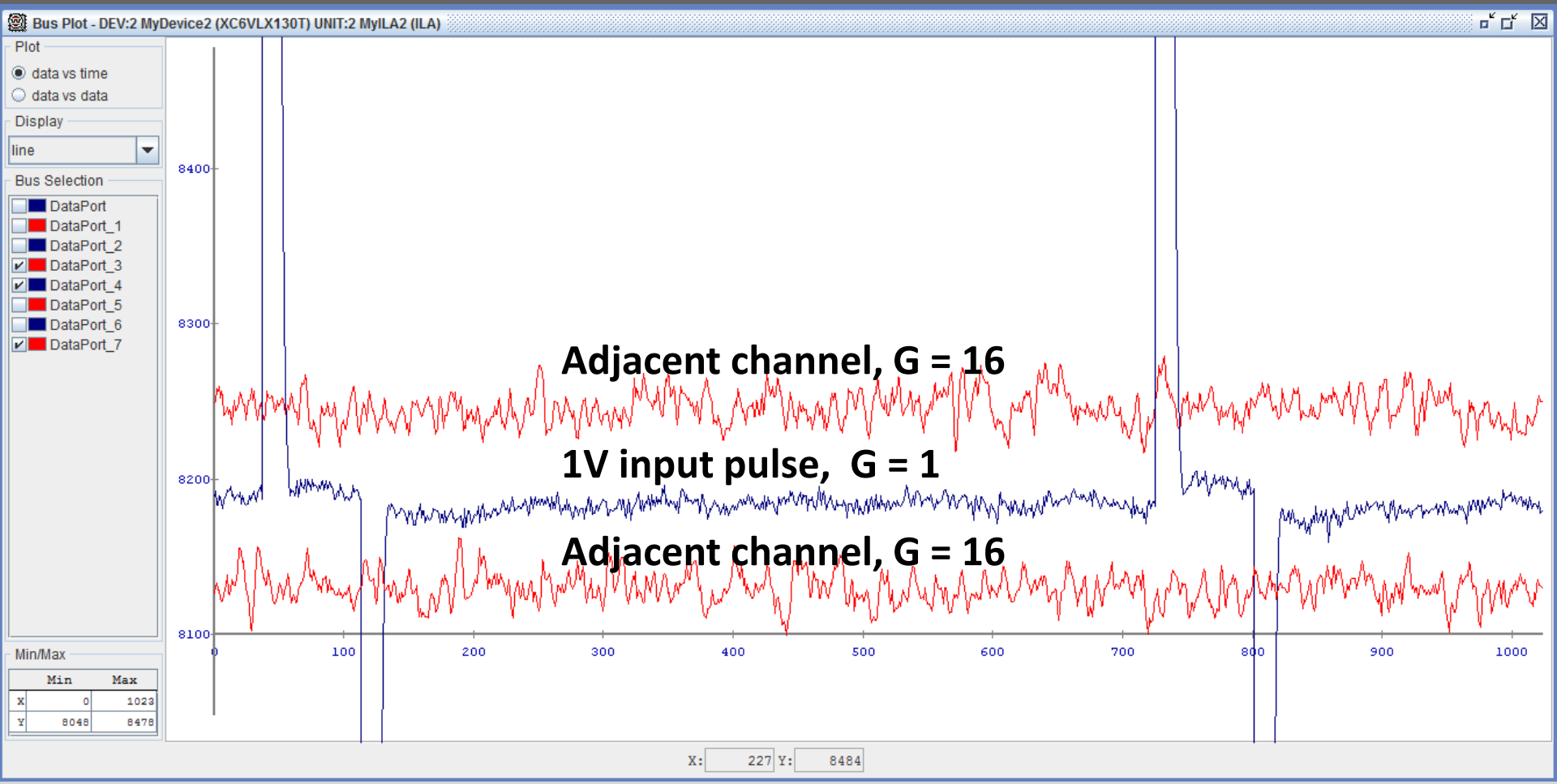
ADC for EMC-Endcap

- 1V pulse - bipolar



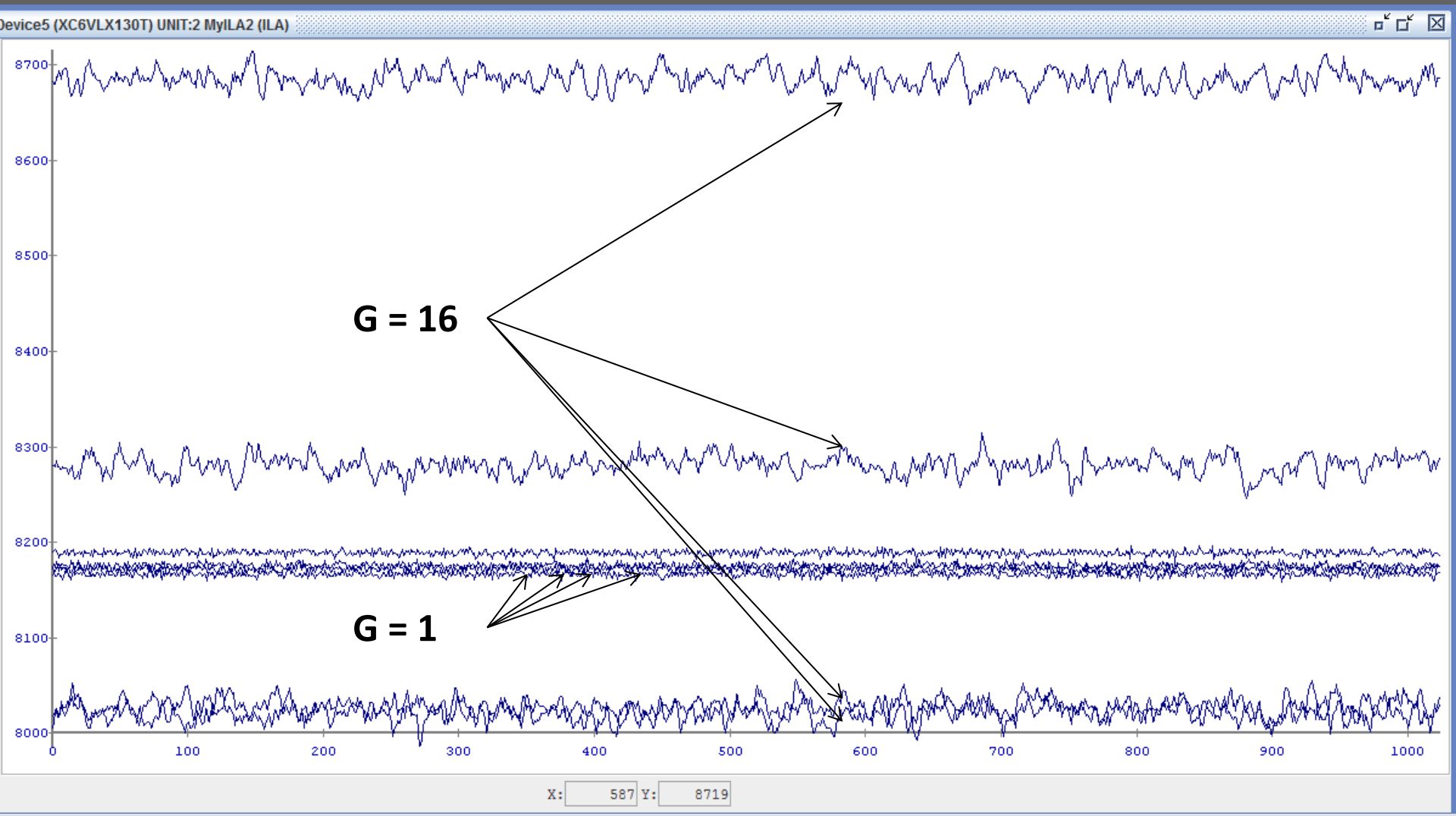
ADC for EMC-Endcap

- Cross-talk



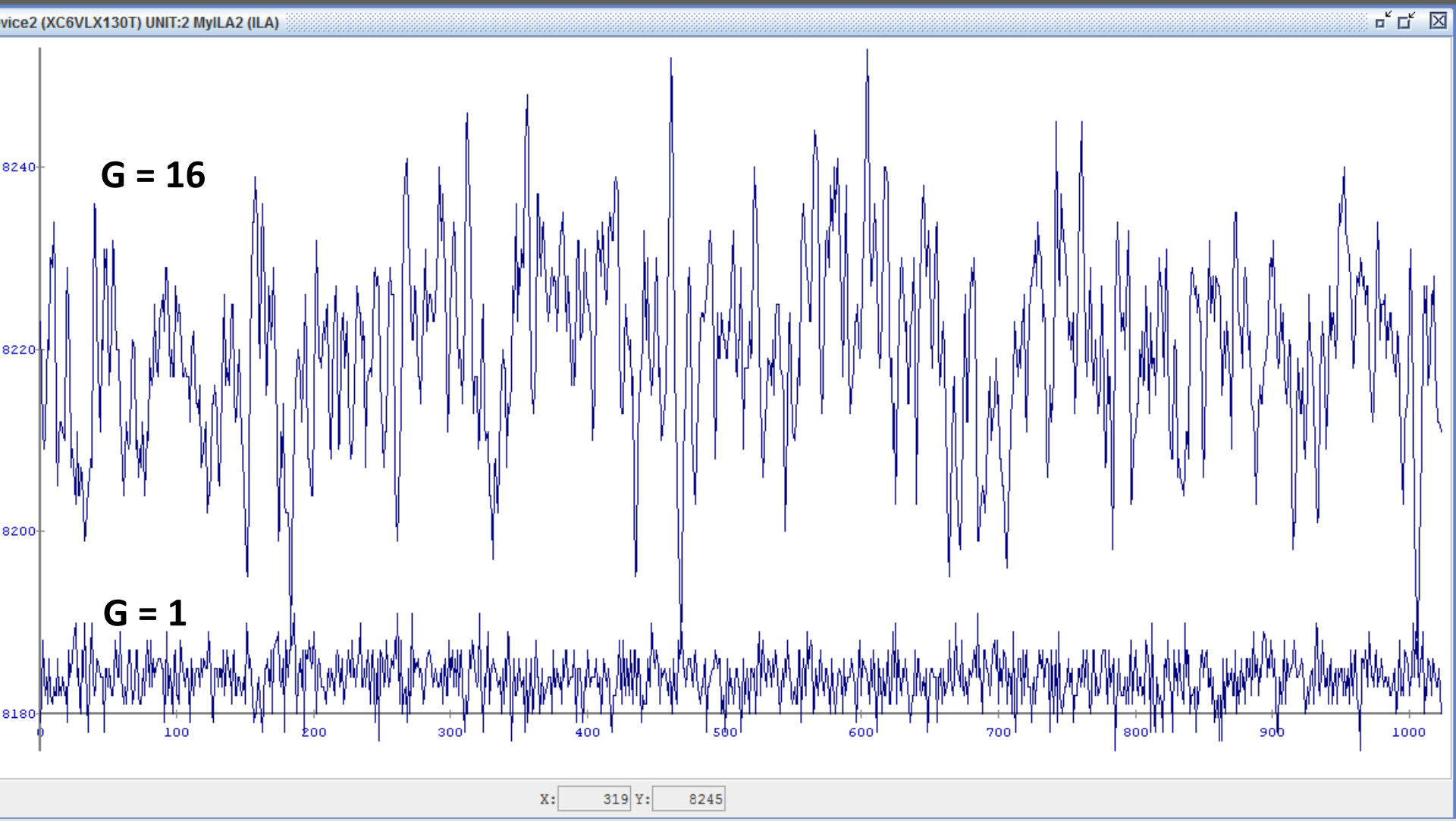
ADC for EMC-Endcap

- Noise tracks

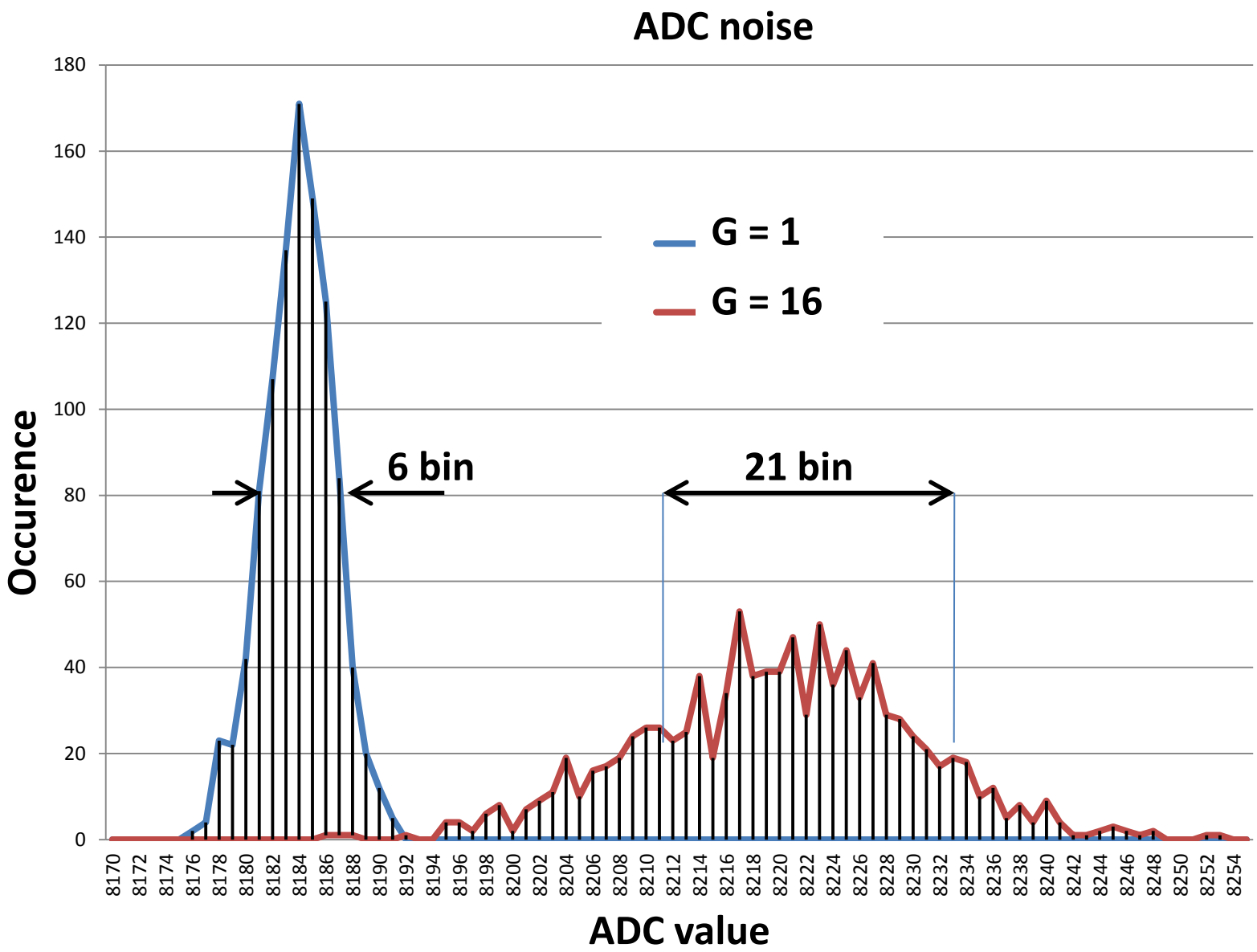


ADC for EMC-Endcap

- Noise track

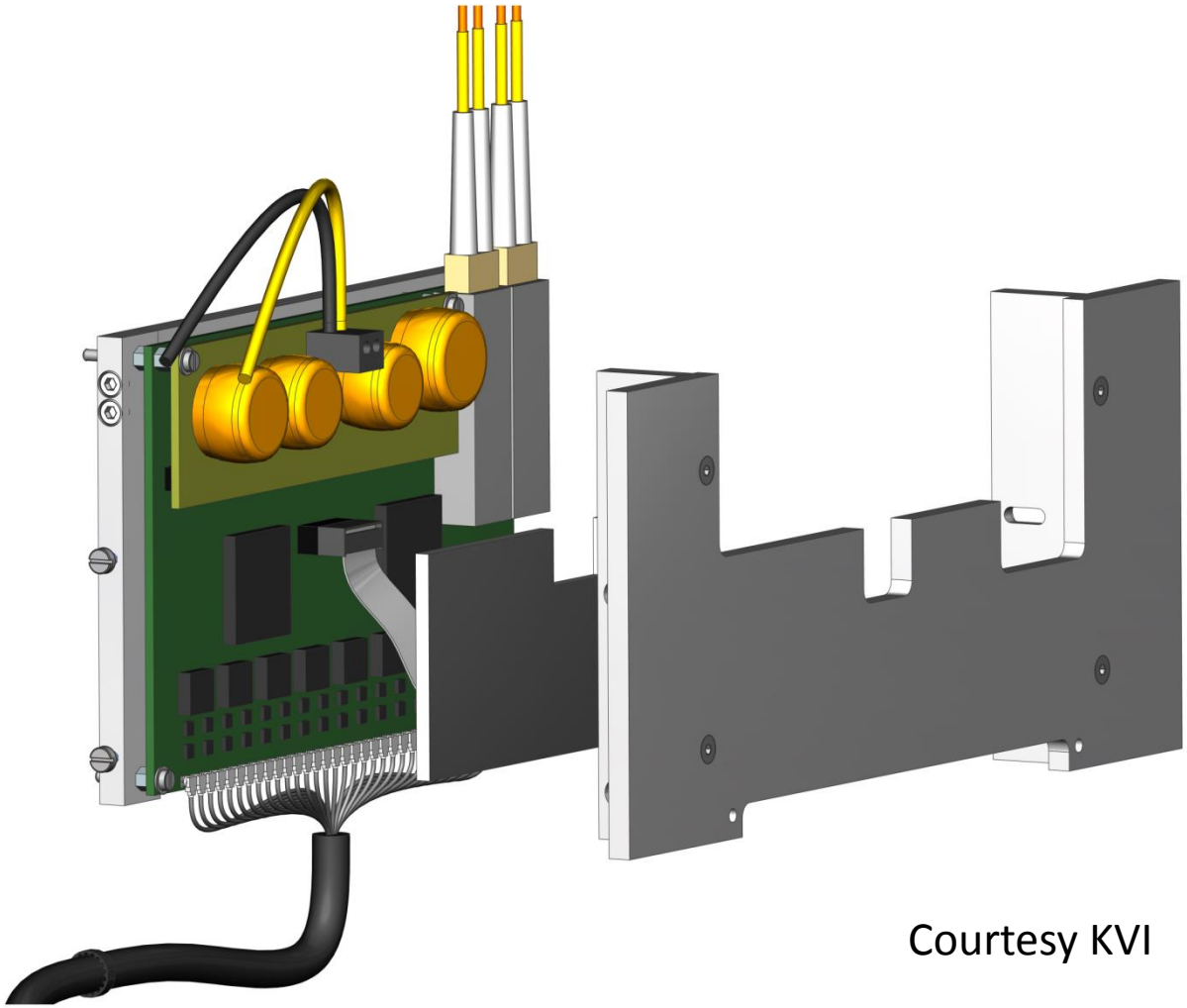


Noise – amplitude spectrum



ADC for EMC

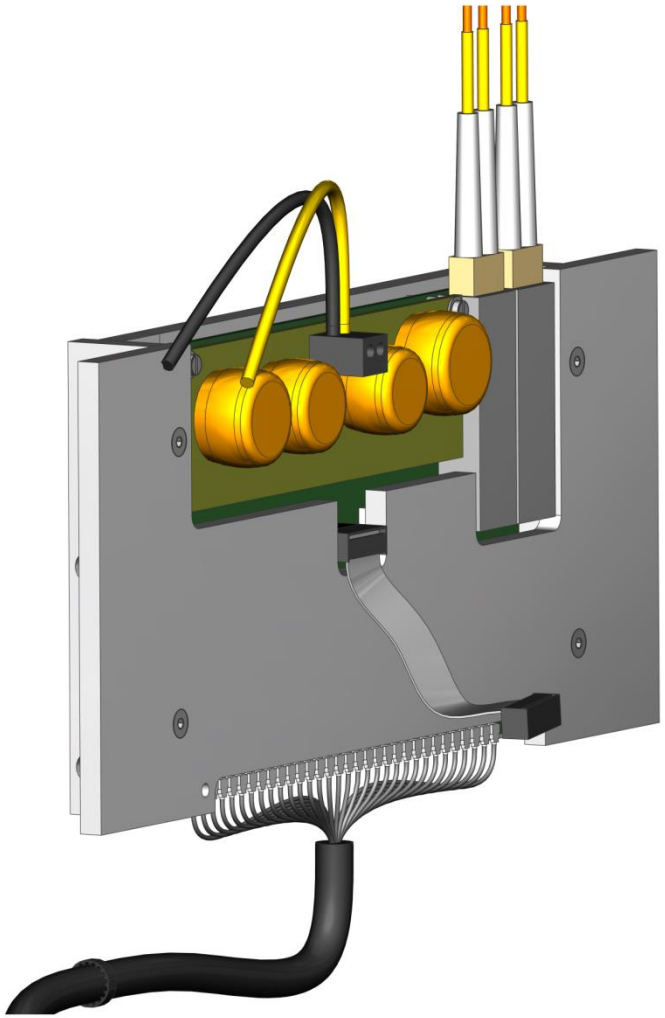
- Encapsulation and Cooling



Courtesy KVI

ADC for EMC

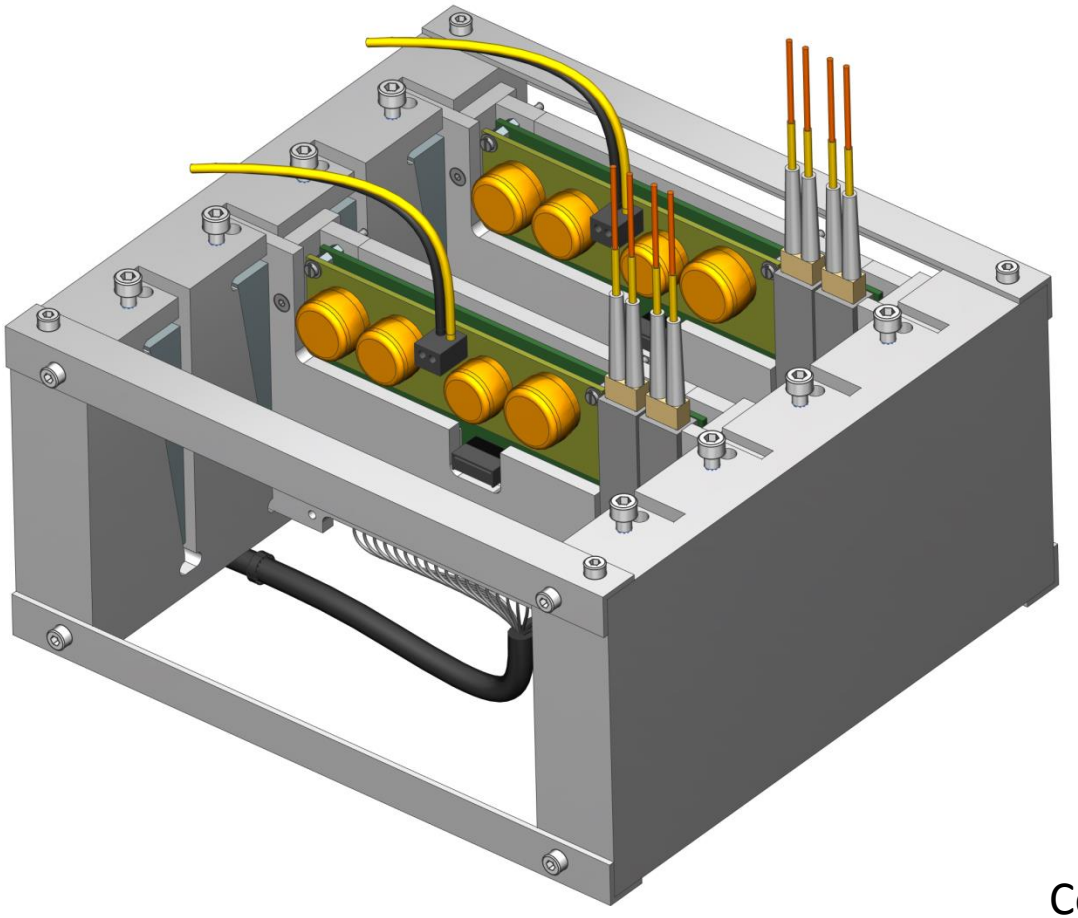
- Encapsulation and Cooling



Courtesy KVI

ADC for EMC

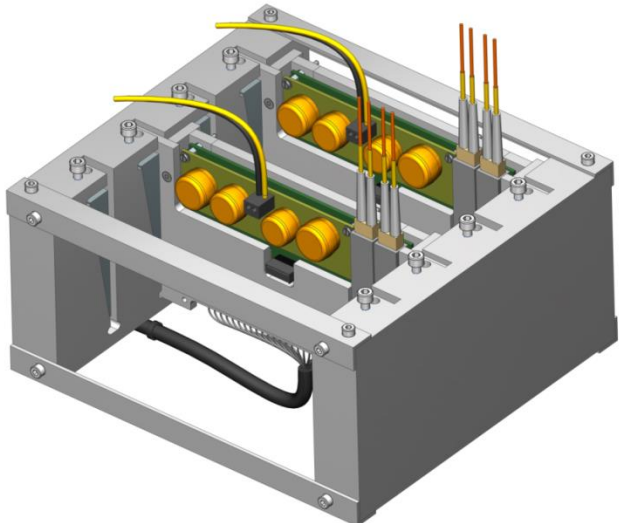
- Encapsulation and Cooling

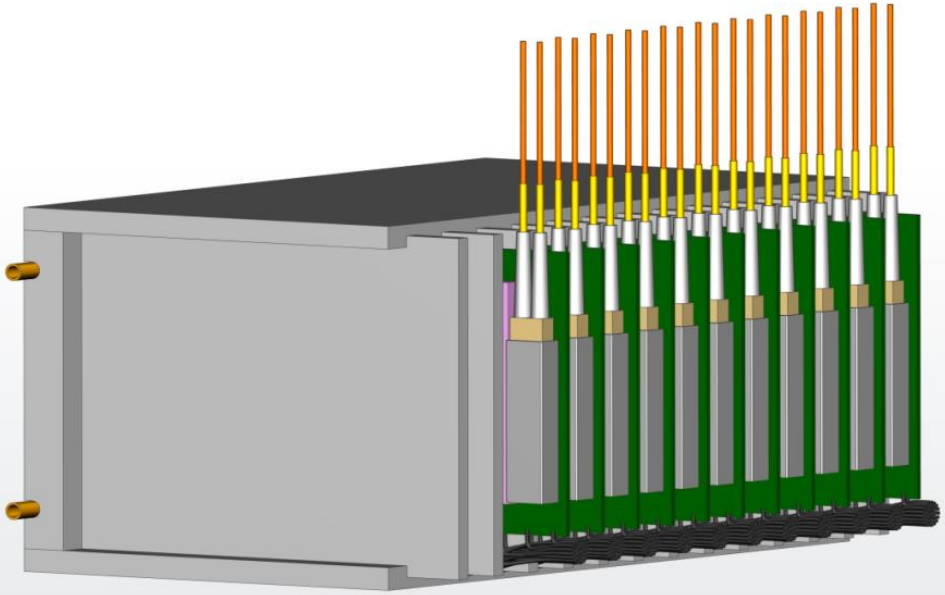


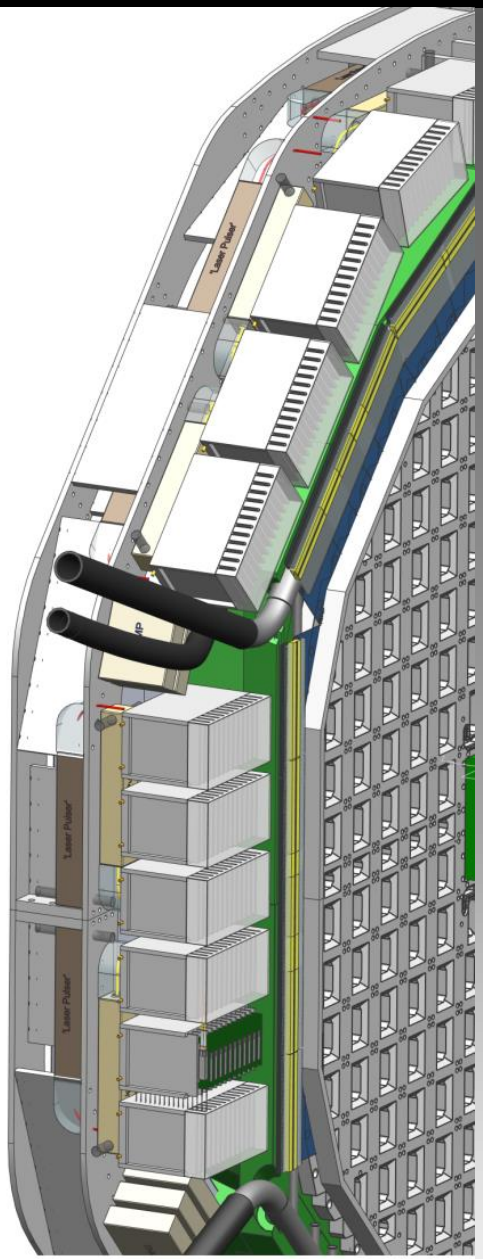
Courtesy KVI

ADC for EMC-Endcap

- Encapsulation and Cooling

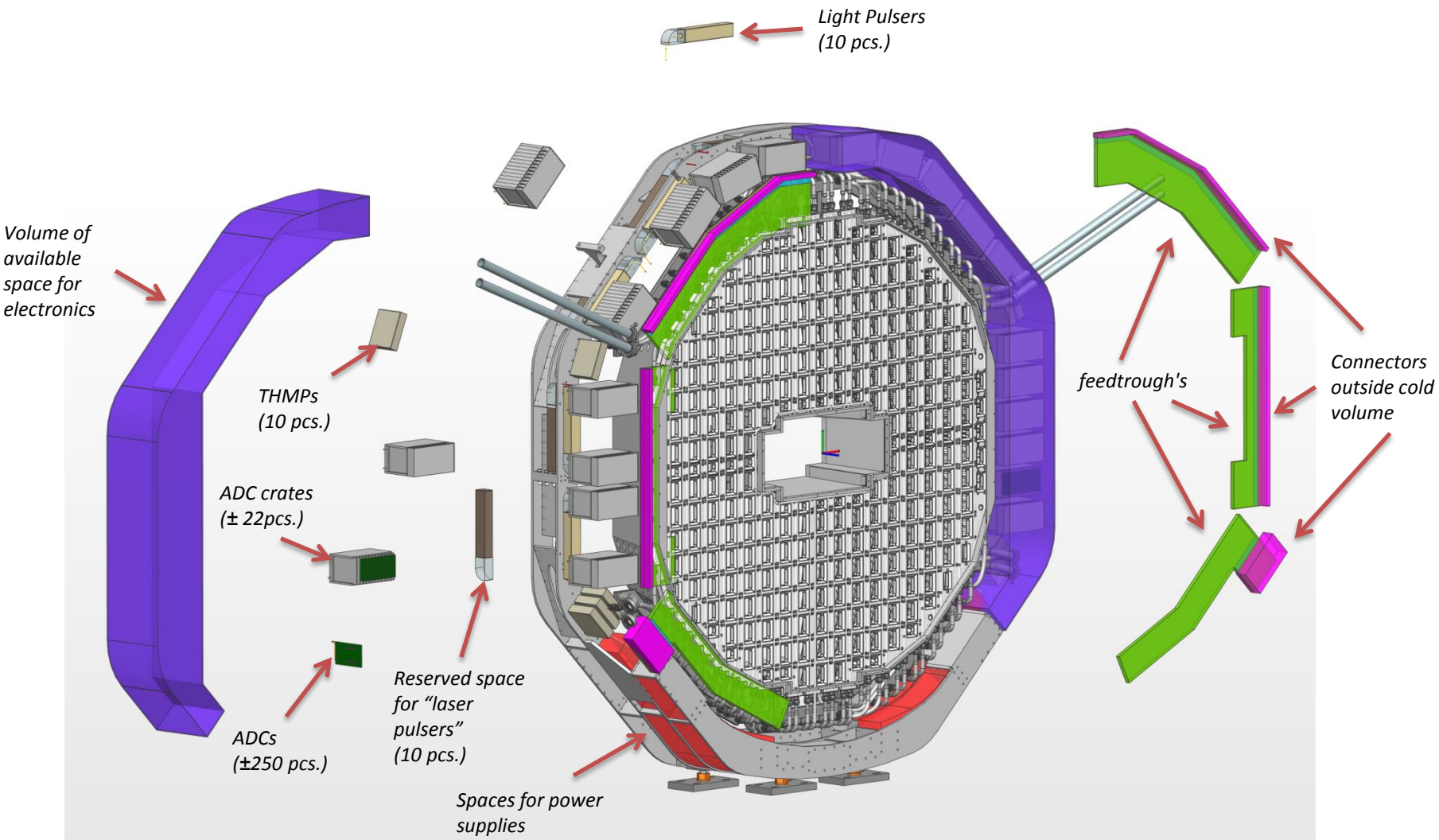






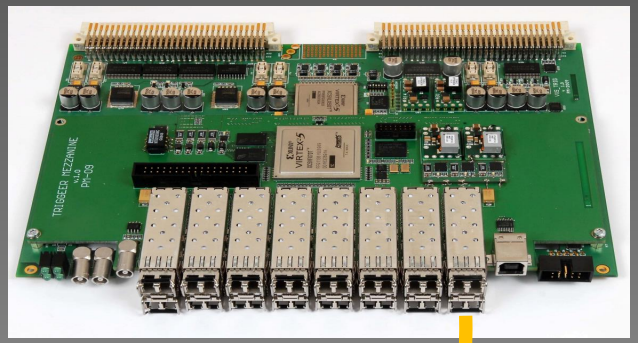
ADC for EMC

- Encapsulation and Cooling



ADC for EMC

- $PbWO_4$/VPTT tests at Max Lab



ATLB (VME Optical Data Concentrator)

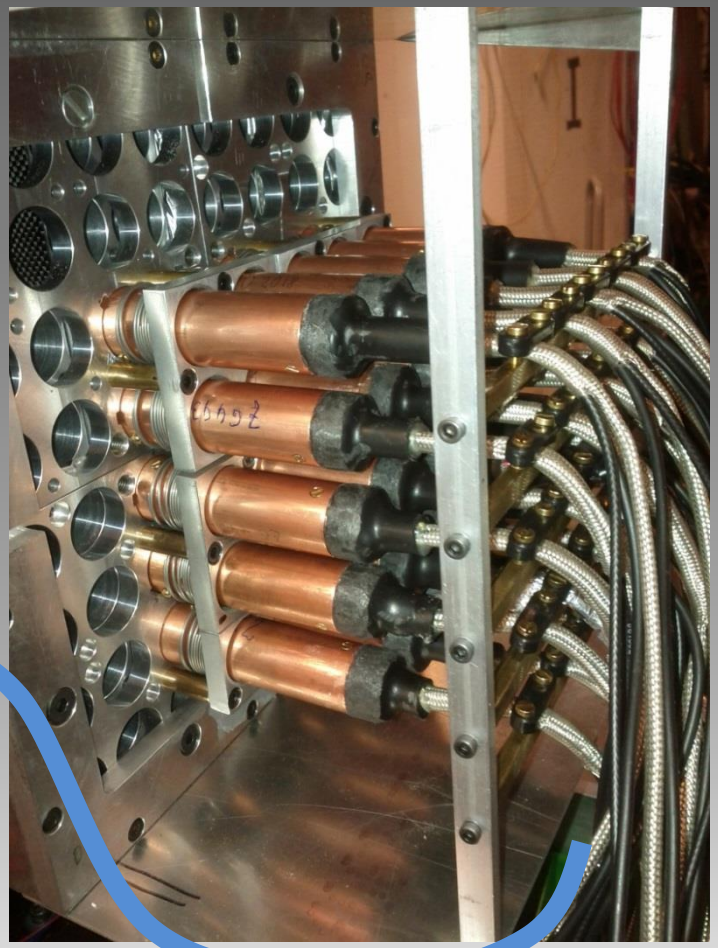
Data Format

Event No
Trigger Time Stamp
Ch. No
Ch. Time Stamp
Ch. Amplitude
Ch. Integral
Ch. Raw Data 0
.
Ch Raw Data 63
Read Word Count

X9

ADC32DR

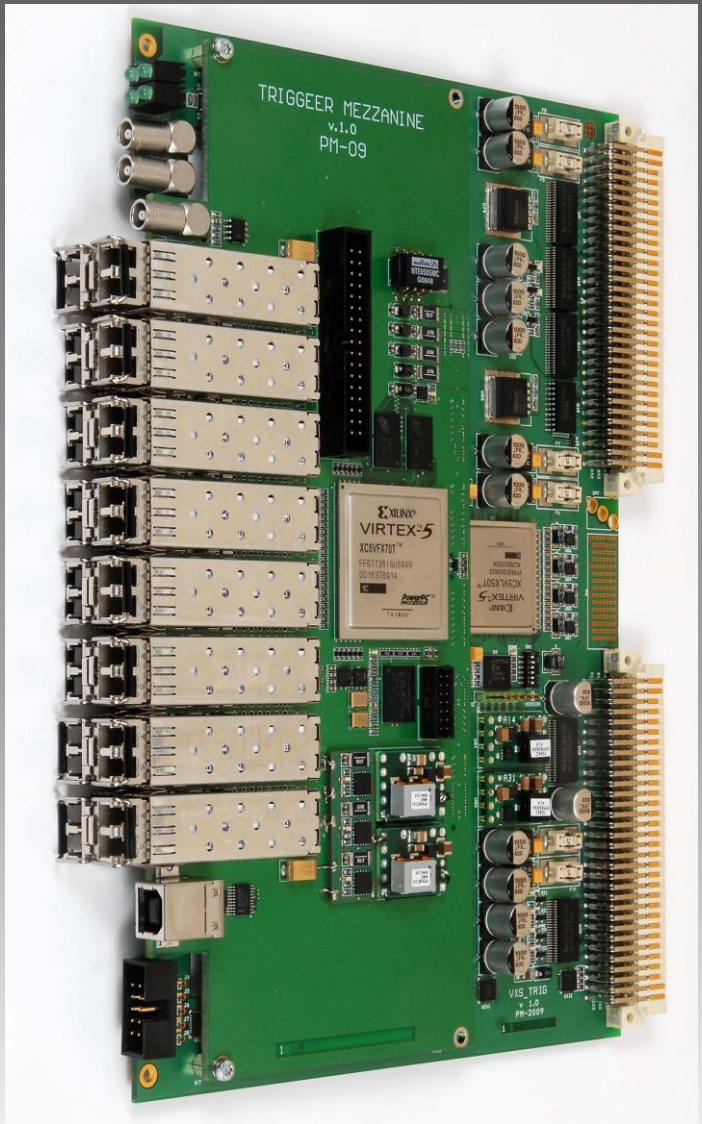
$PbWO_4$ + VPTT
100uV/MeV



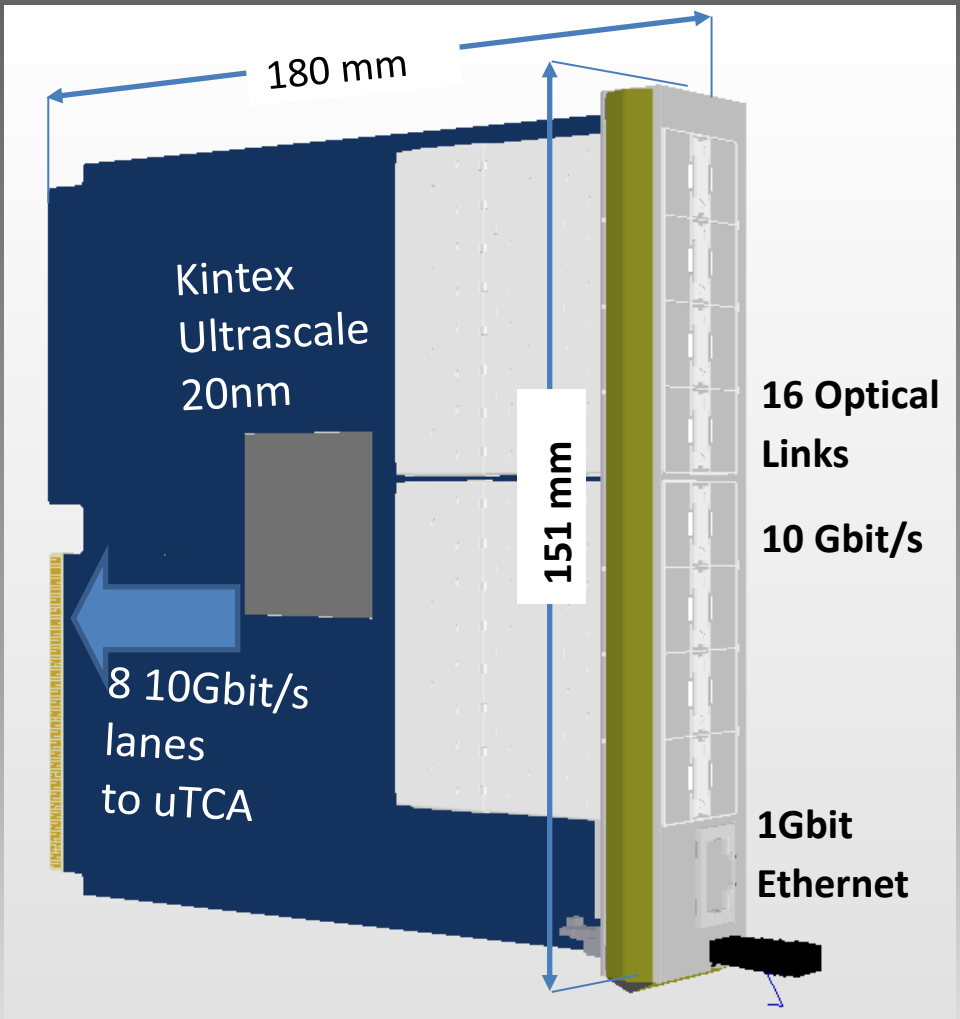
ADC for EMC

- Data Concentrators

VME64x

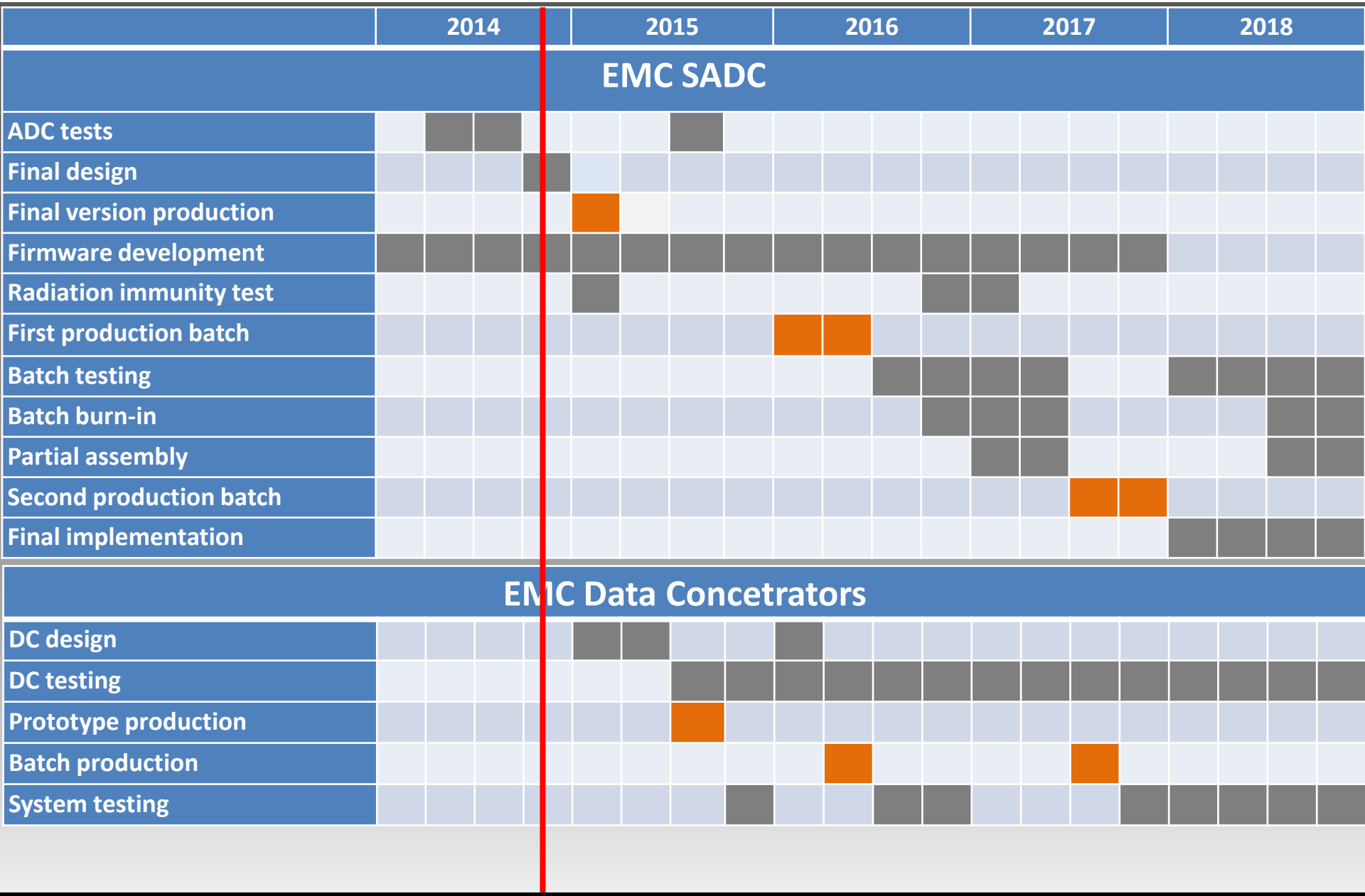


AMC (uTCA)



ADC for EMC

- Schedule



Manpower

Uppsala

Hardware design	- Pawel Marciniewski
System integration	- Postdoc

Stockholm

Firmware	- PhD

KVI Groningen

Firmware	- Peter Schakel

Uni Bonn

Firmware/Integration	- PhD (Johannes Muellers)

Thank You !