Challenges and opportunities for a First Level Trigger based on Silicon Trackers for the High Luminosity LHC

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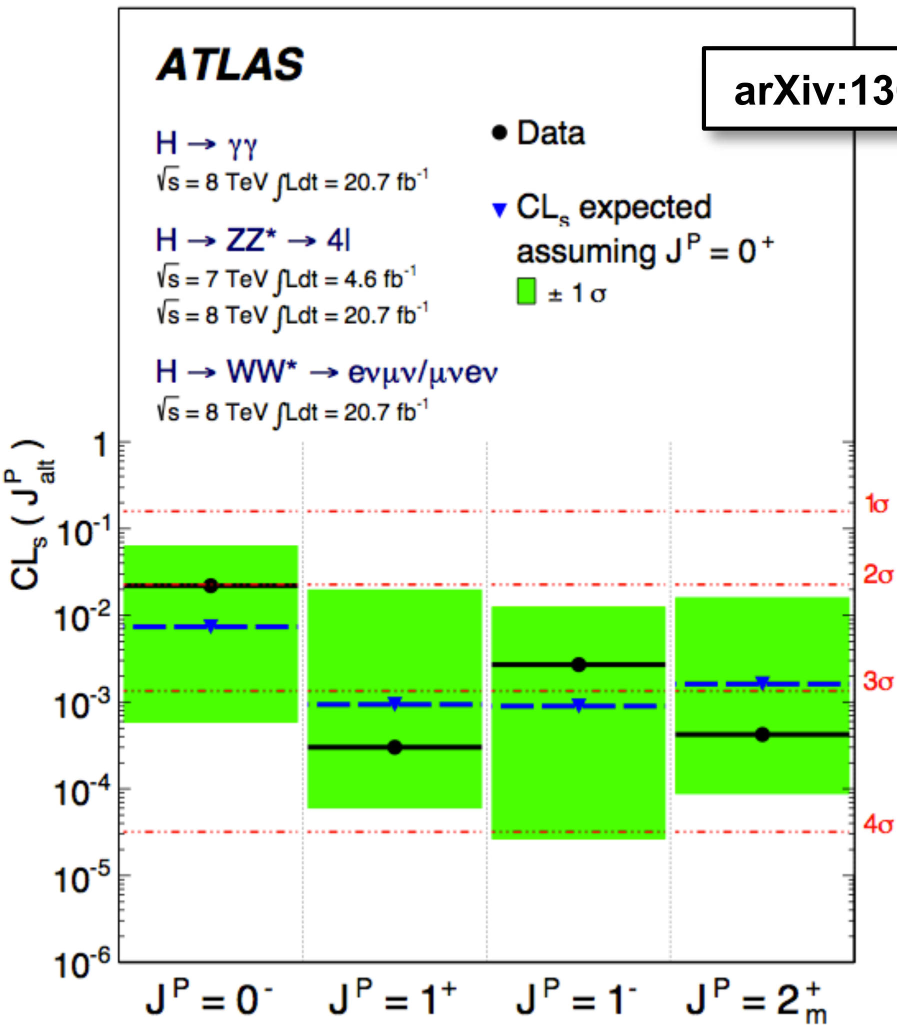
Run1 legacy

Higgs-like particle has now become a (the) Higgs boson

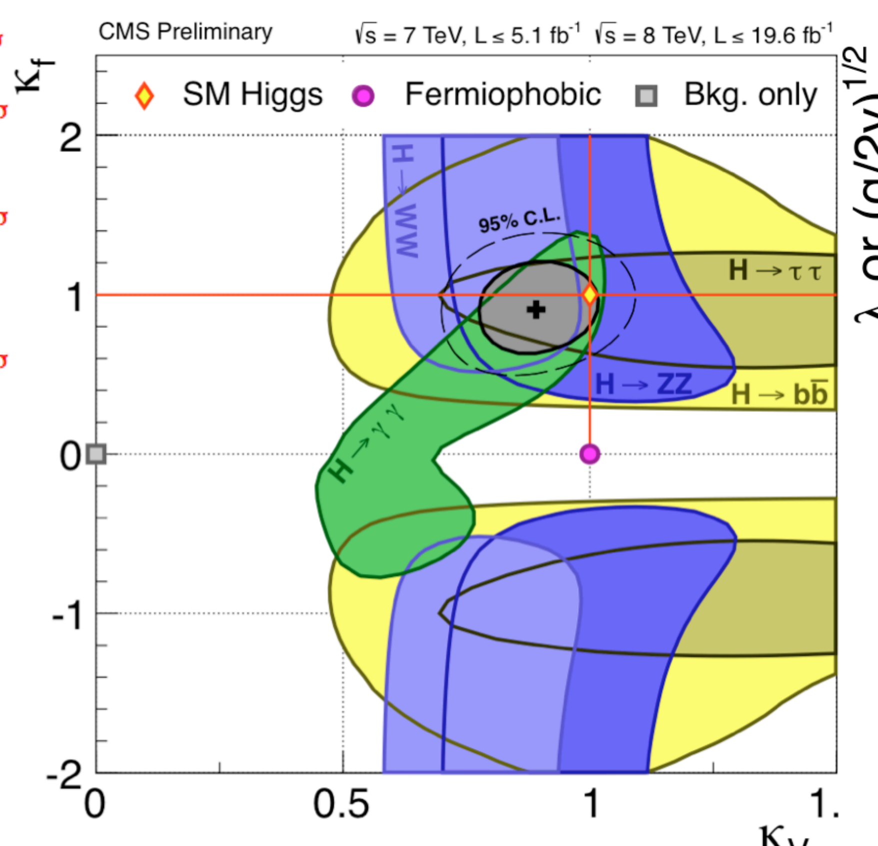


arXiv:1307.1432

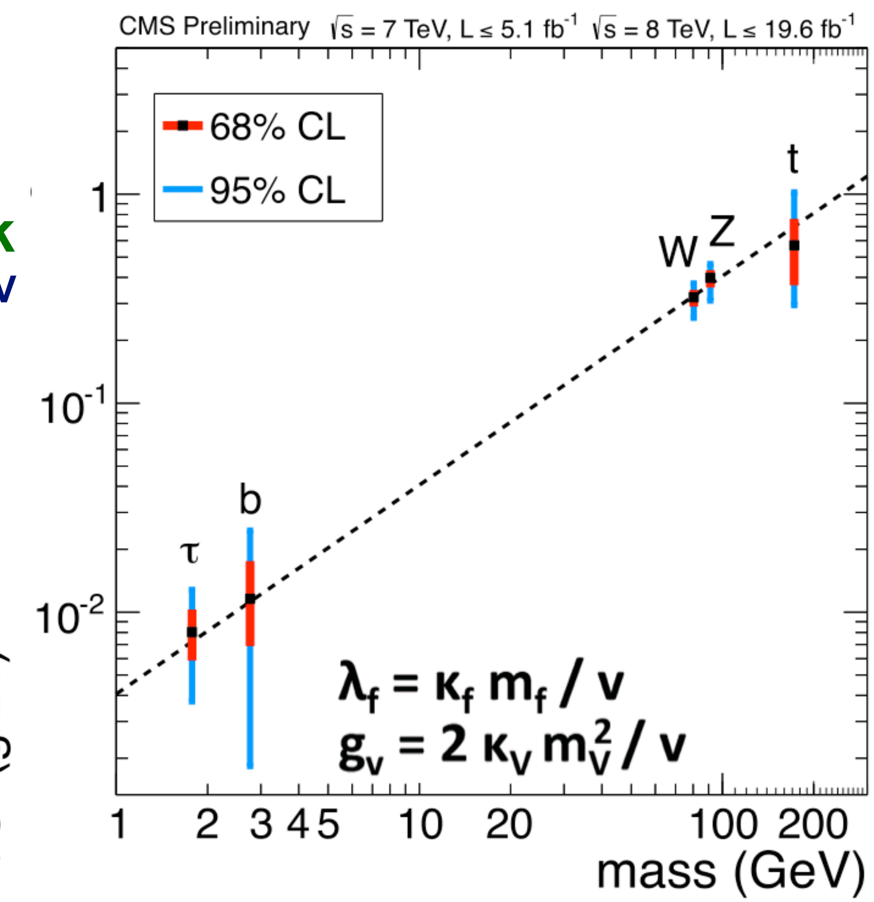
$J^{PC} = 0^{++}$ strongly favored over alternative hypotheses

Higgs mass already measured more precisely than top quark

ATLAS: m(H) = 125.5 ± 0.2 $^{+0.5}_{-0.6}$ GeV
CMS: m(H) = 125.5 ± 0.3 ± 0.3 GeV



Vector and fermion couplings grouped together



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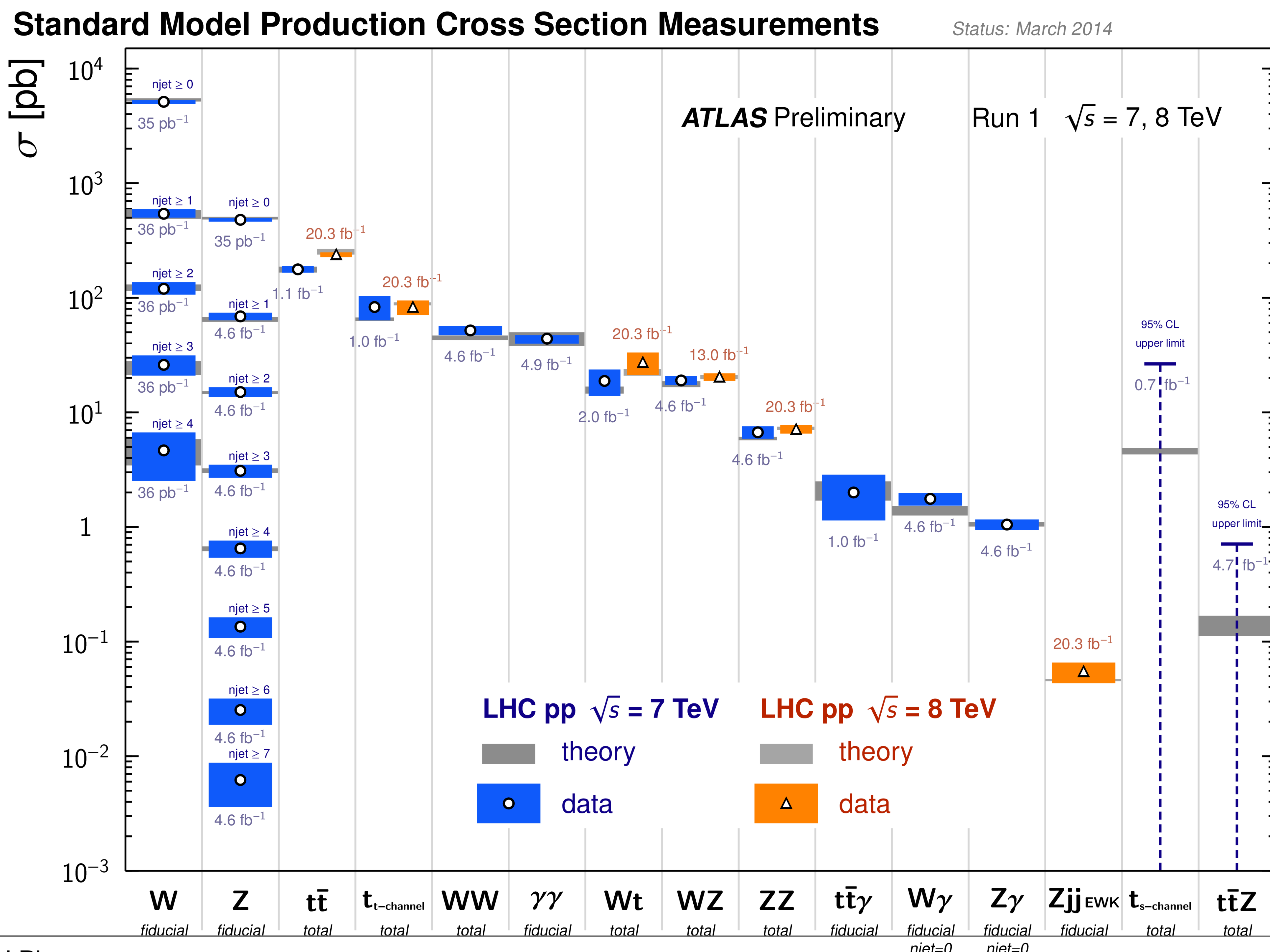

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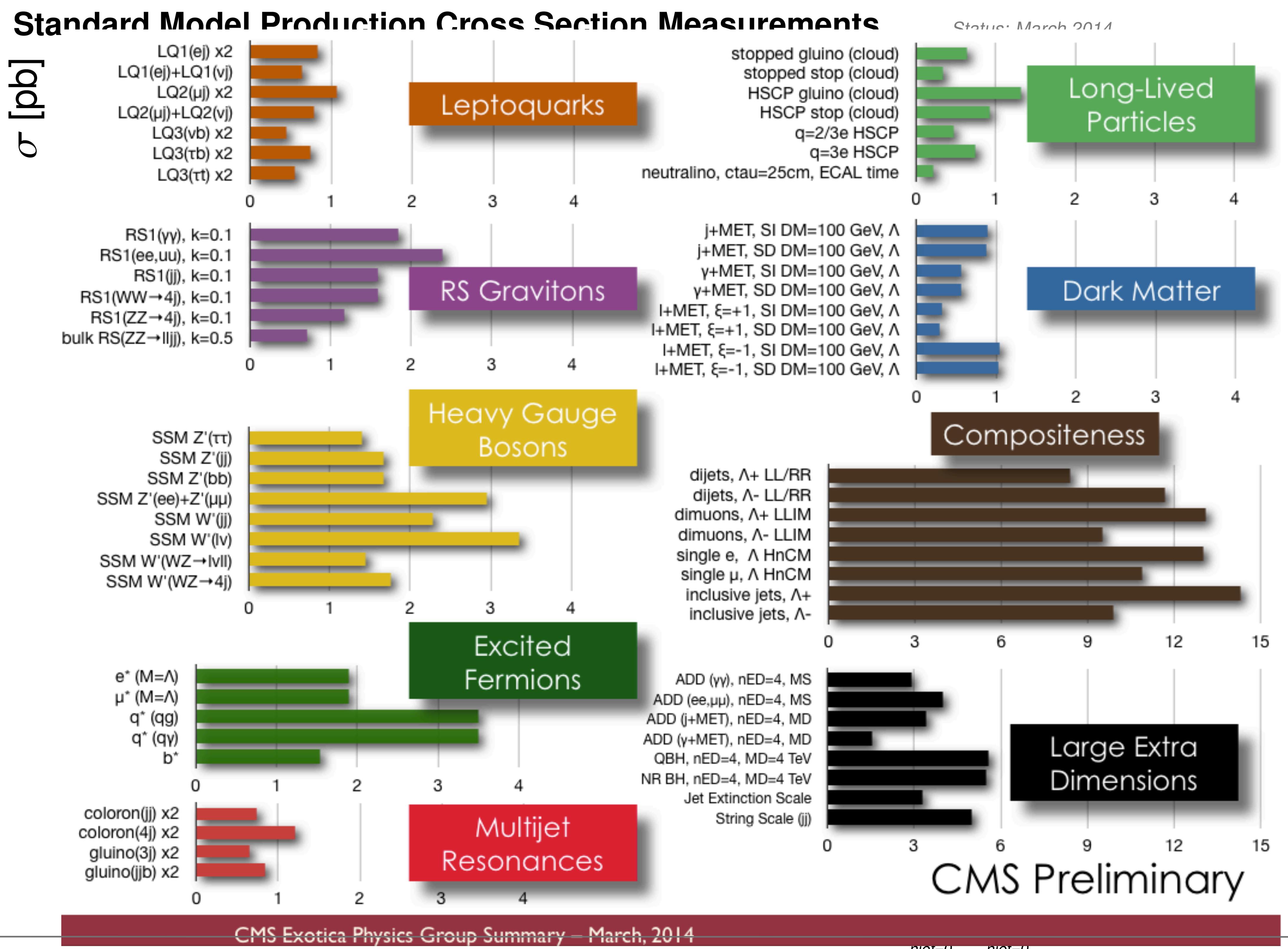

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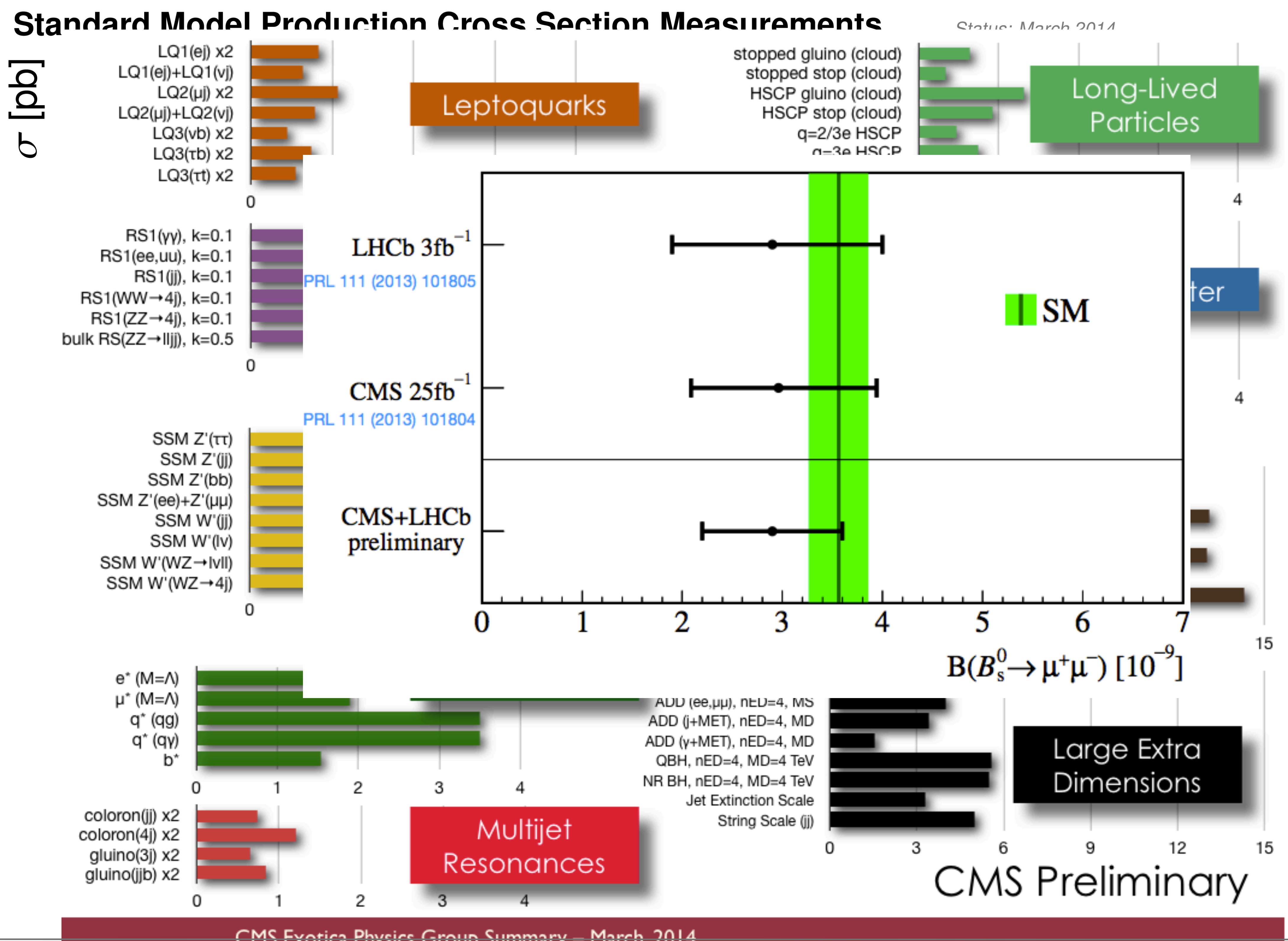

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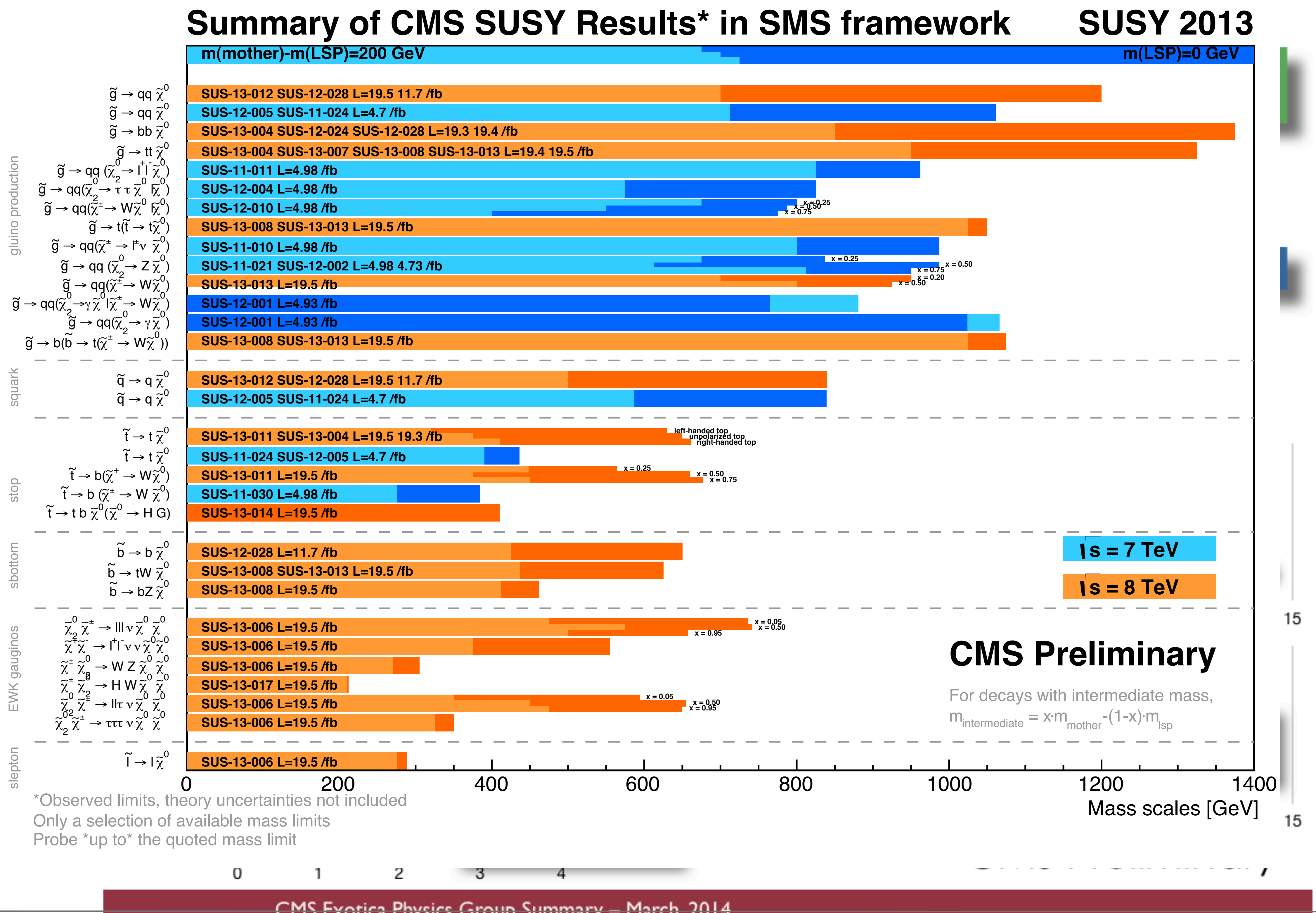
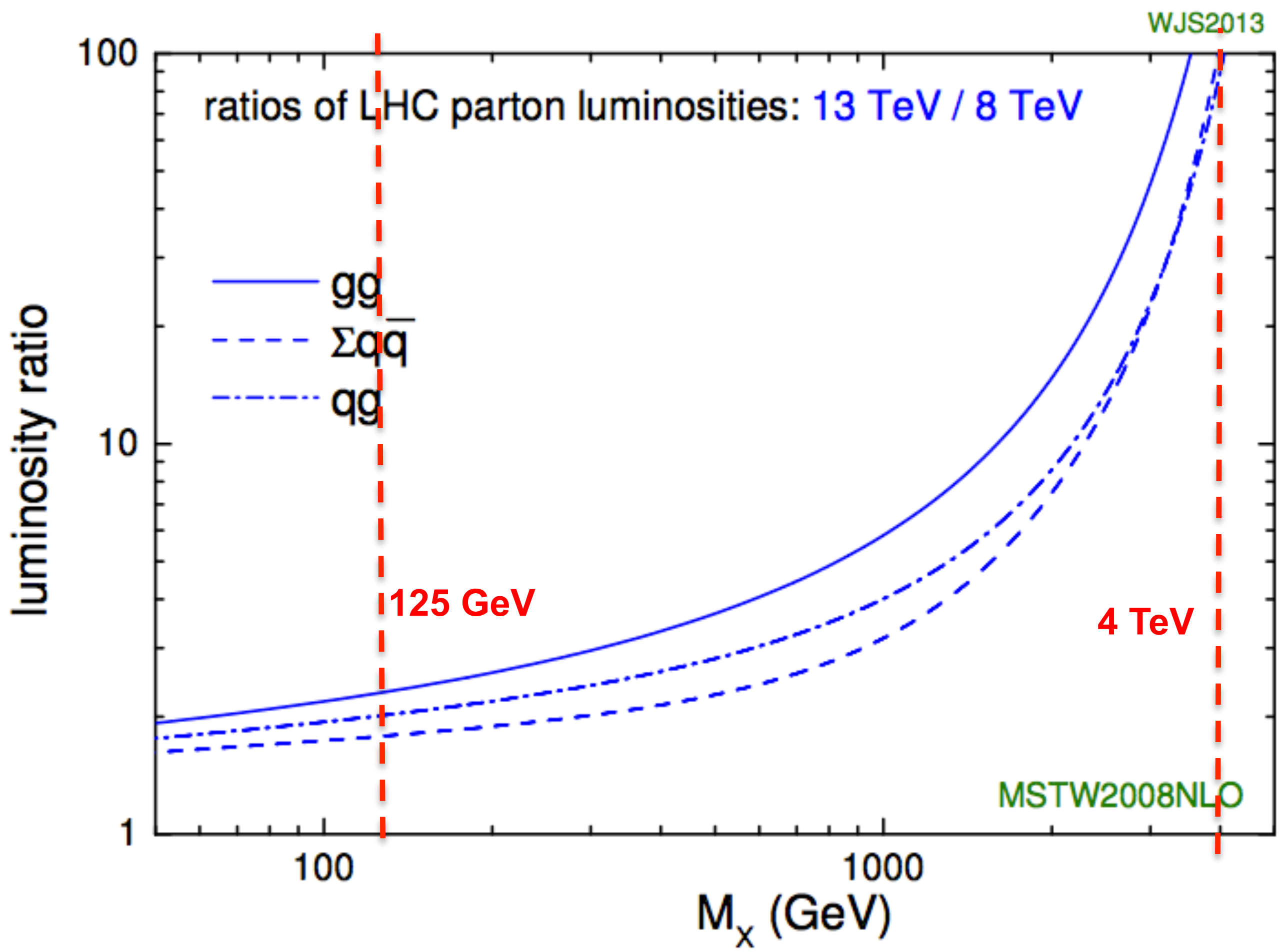
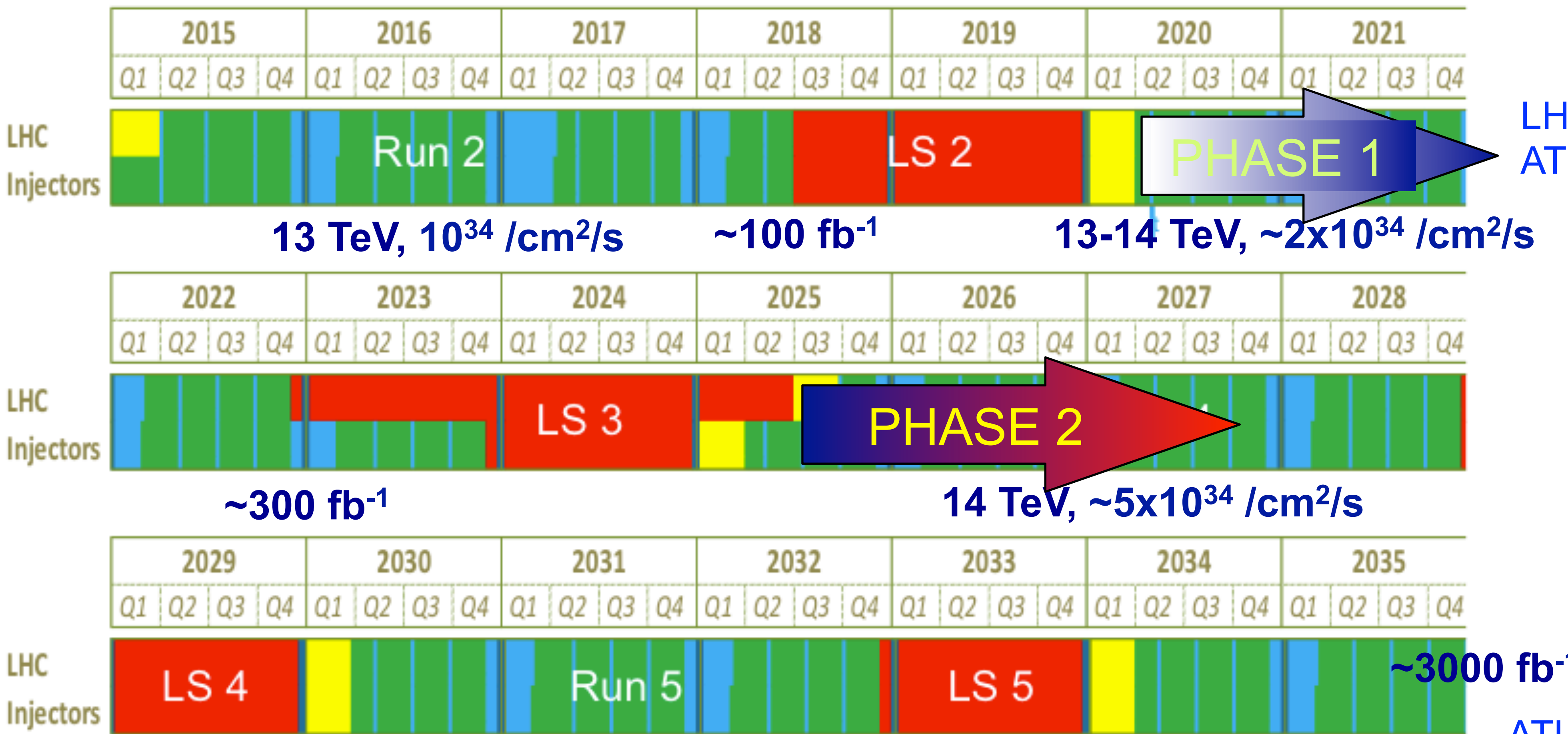


What could be done next?

- Run 2 (2015-18):
  - ~100 fb^{-1} at 13 TeV, 10^{34} cm^{-2} s^{-1}
    - Gain depends on coupling (qq, gg, qg)
      - 1 year worth ~250 years of 8 TeV data for e.g. 4 TeV Z' or 2 TeV squarks big gains in sensitivity



The HL-LHC scenario



LHCb Upgrade
ATLAS/CMS Upgrades phase 1

HL-LHC
14 TeV
>250 fb-1/year

ATLAS/CMS
Upgrades phase 2

At HL-LHC ~140 events/bx spread over ±15 cm (3 σ)

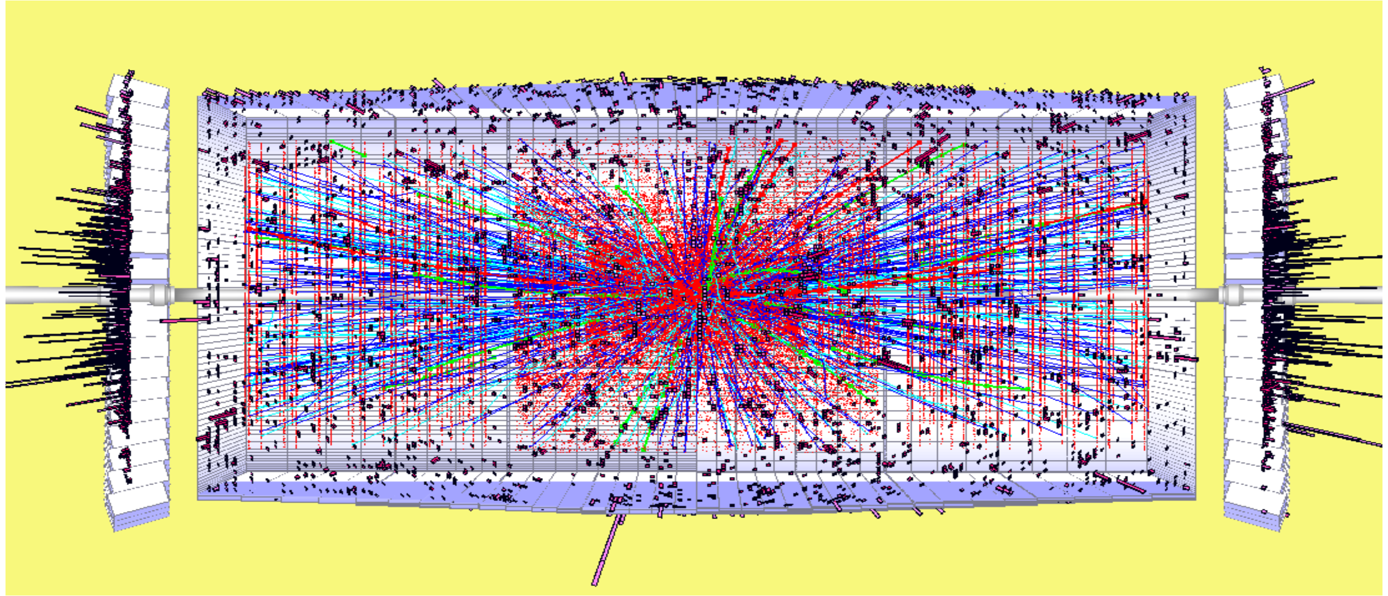
~3000 fb^{-1} expected in 10 years running

Excellent opportunity to search for (rare) and new phenomena

Need anyway still to trigger on “SM” objects (leptons, b, jets, MET)

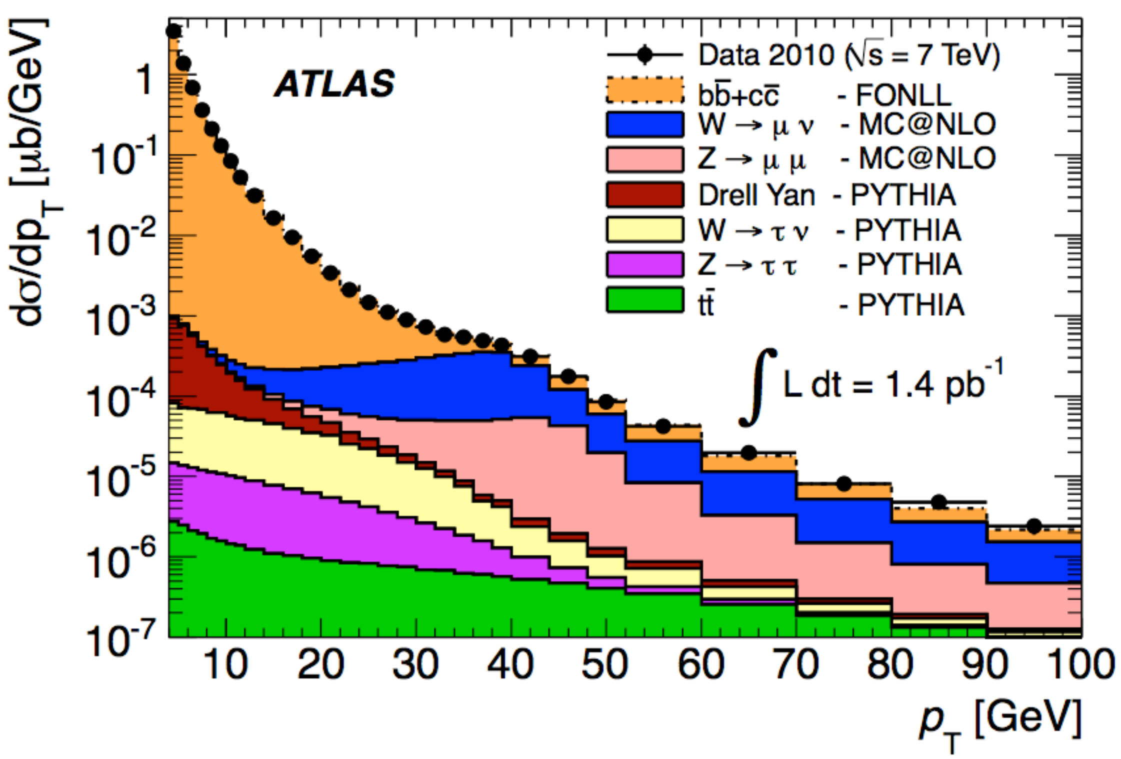
Implications for the Trigger

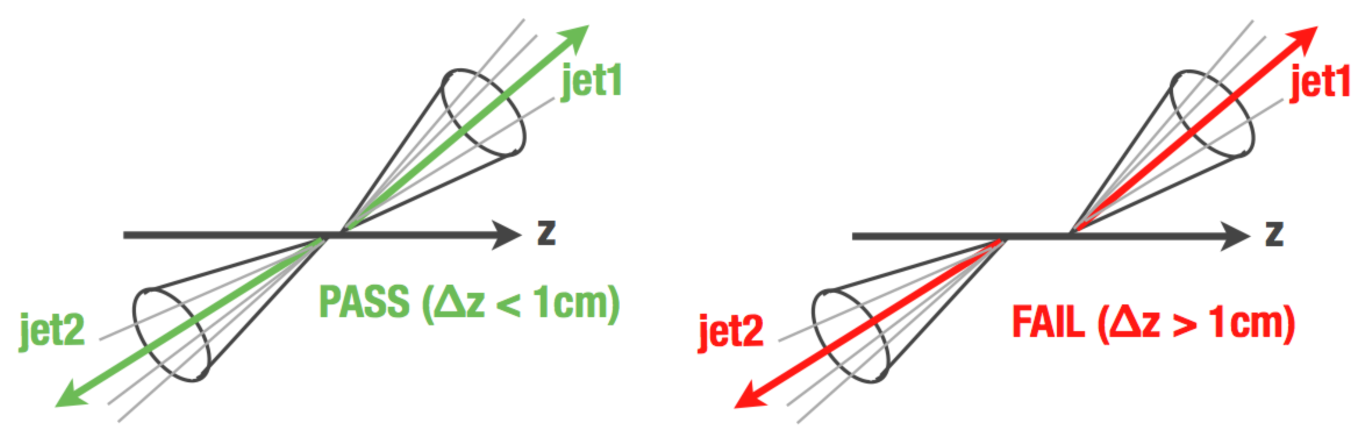
- At 5×10^{34} cm^{-2} s^{-1} up to ~140 interactions per bunch crossing
  - About 6k primary tracks per bunch crossing in the Tracker volume $|\eta|<2.5$ ...
    - ...plus any other coming from γ conversions and nuclear interactions
  - ~ one order of magnitude larger wrt LHC
  - Severe Triggering conditions
    - Too many primary vertices, need to have smarter triggers combining information from several subdetectors
    - Need to maintain low thresholds for basic objects, even with an increase in the L1-Accept bandwidth (currently at 100 kHz)
  - Both ATLAS and CMS will replace their "inner trackers" to cope with the nasty environmental conditions
    - The usage of the Tracker would help to disentangle among those 140 pileup events



Why a Track Trigger at L1

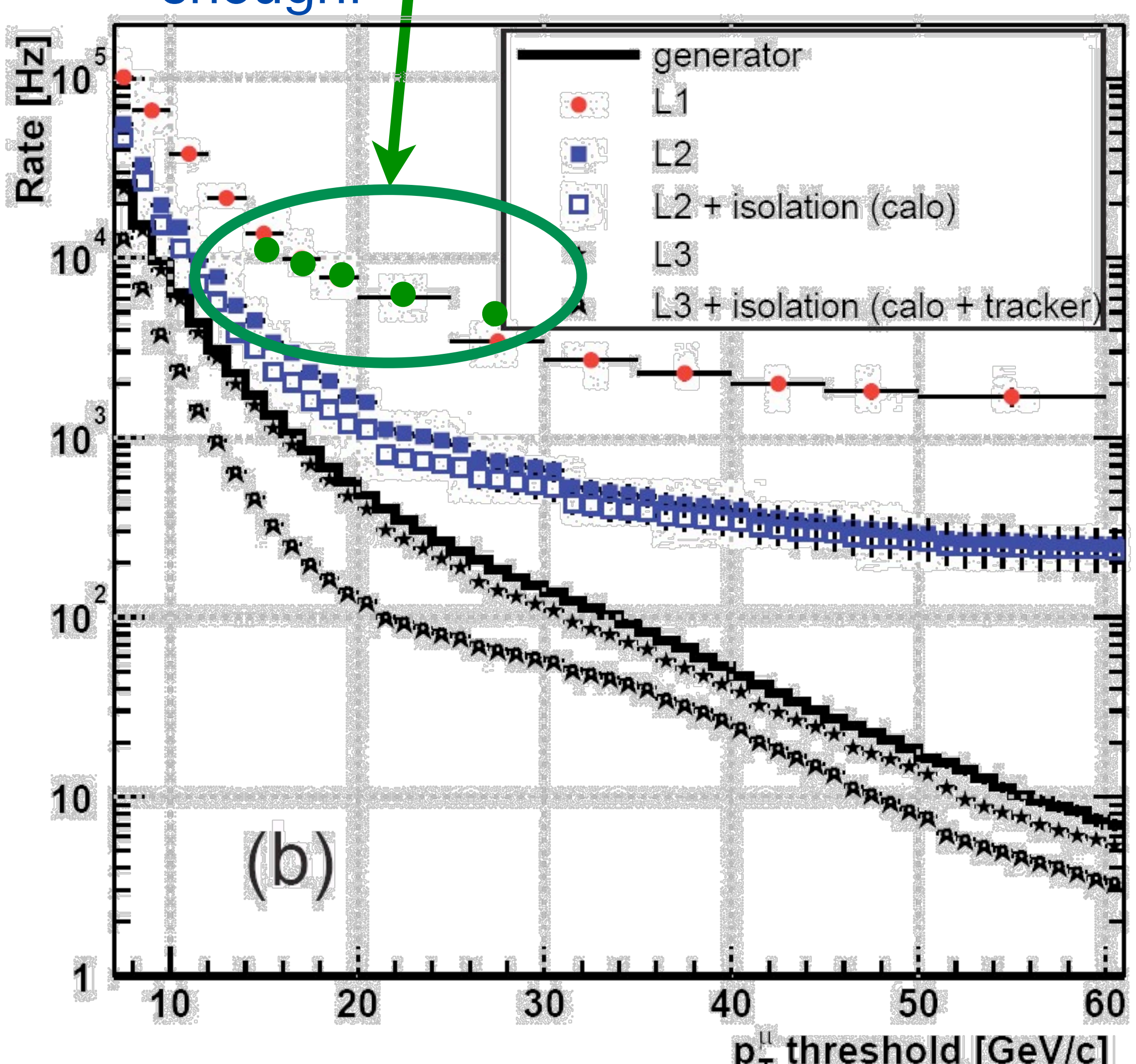
- HL-LHC physics goals require excellent Trigger selectivity on basic objects (leptons, jets, taus, b-jets, MET)
  - This might be jeopardized by the increased level of pileup events (140 on average)
    - Huge rate of μ from heavy flavors ⇨ use better p_T resolution from tracker
    - Prompt electrons at L1 need to be separated from huge γ ⇨ Tracker tracks
    - High E_T jets from (many) different primary vertices ⇨ jet-vertex association
    - Photon isolation in Calorimeters compromised by large pileup ⇨ use tracks



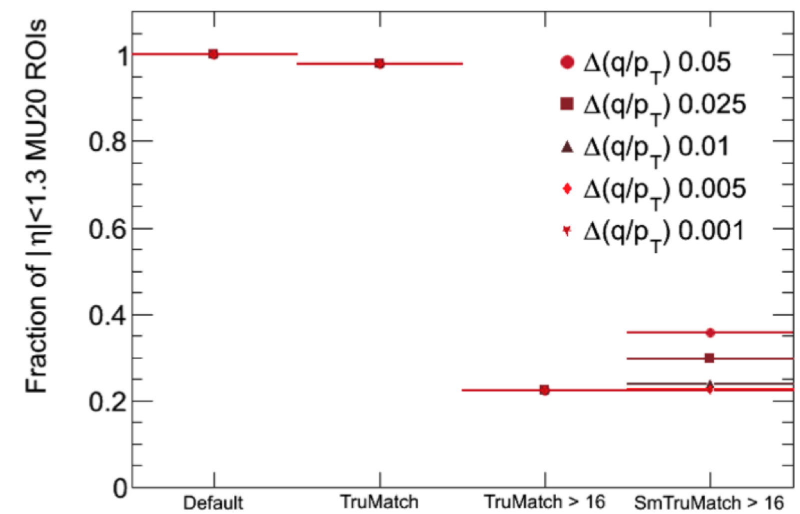


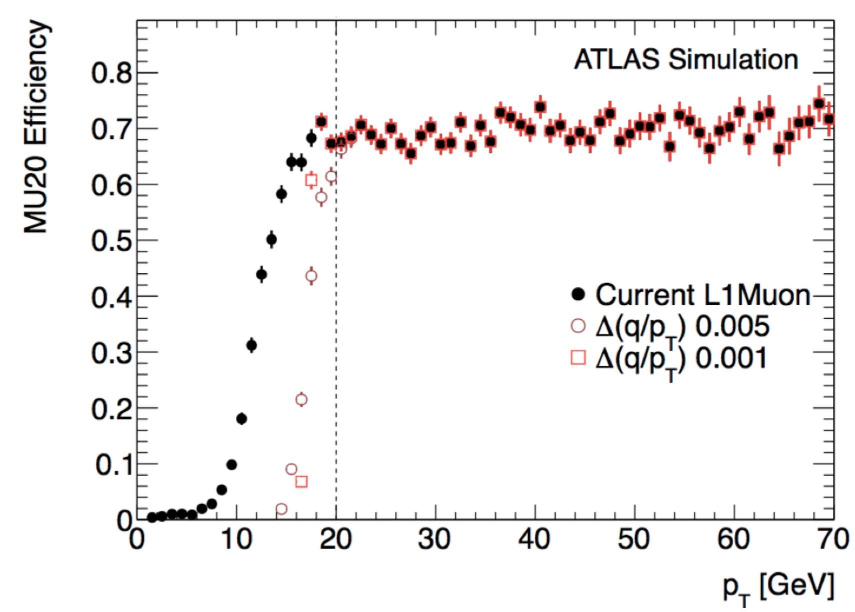
Examples from ATLAS and CMS

- CMS simulation for $L=10^{34}\ cm^{-2}\ s^{-1}$
- Add measured data rates at 8 TeV, extrapolated to $10^{34}\ cm^{-2}\ s^{-1}$
  - No p_T threshold may reduce the rate enough!



- ATLAS simulation
  - ~80% of μ originate from lower p_T
  - Sharpening the p_T to reduce the rate at constant efficiency





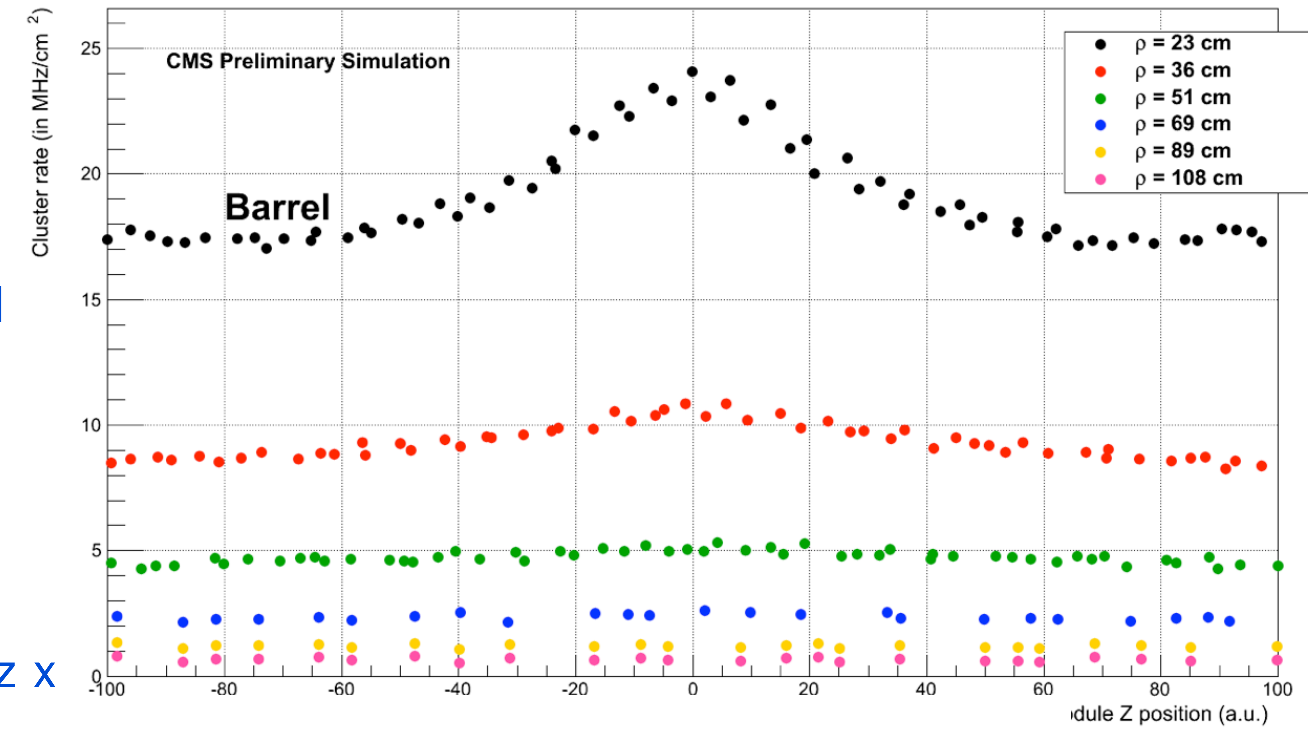
The challenge and the way out

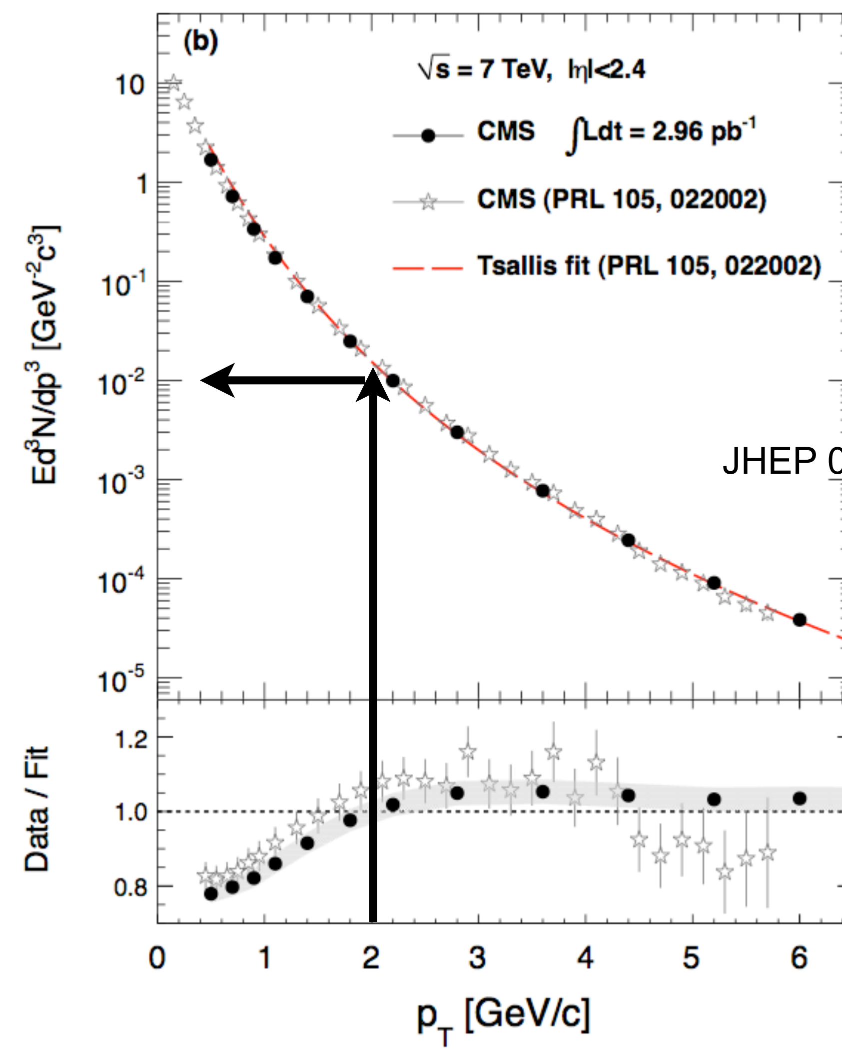
- Take data off the tracker
  - ~ 4k primary tracks within |η|<2.5
    - Large data rates (up to 25 MHz/cm^2)
      - huge contribution from nuclear interactions and photon conversions
    - ~1.3 events/mm × Gauss(σ=4 cm)
    - Short L1A trigger latencies (10-20 μs)
    - Cannot read all (~60 M strips) channels at 40 MHz
      - Even a 1% occupancy: 0.5 M channels x 40 MHz x 20 bit = 400 Tb/s

        ~120k links at 3.25 Gb/s (GBT) - Current CMS Tracker has 40k links (320 Mb/s)
      - Need to

        suppress hits from low p_T tracks

        read at smaller (affordable) rate
- Once data are off-detector, find tracks and
  - formidable pattern recognition problem
    - need latencies of ~5 μs

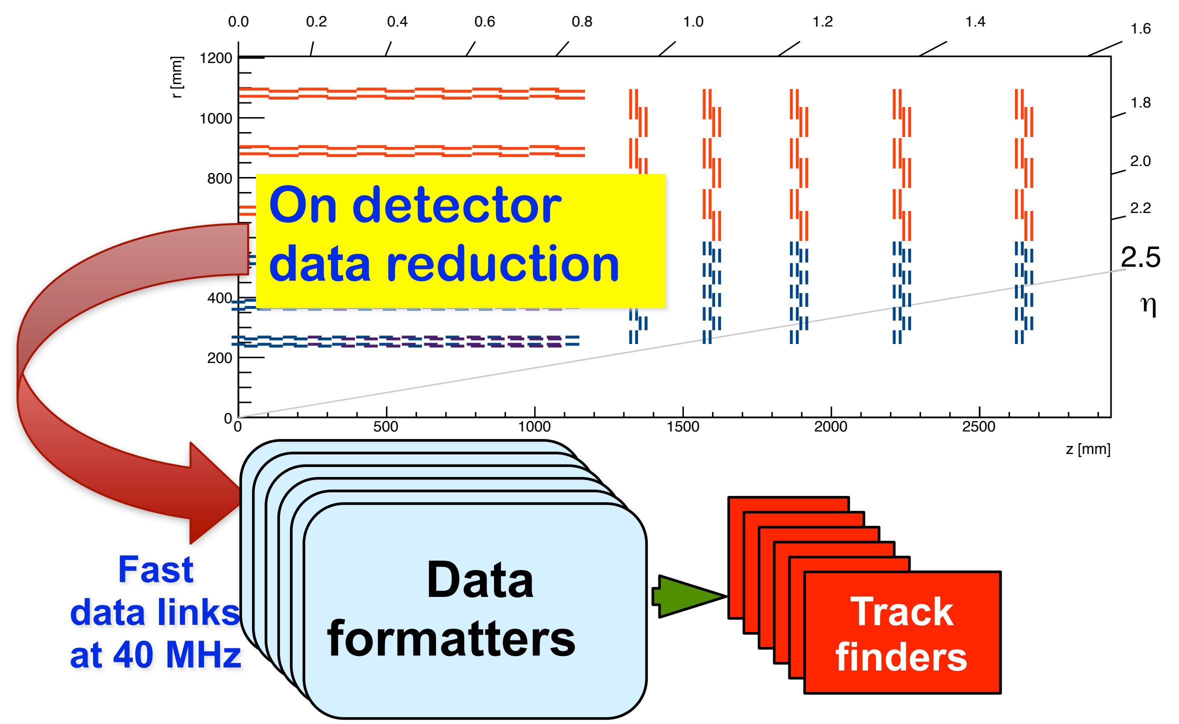


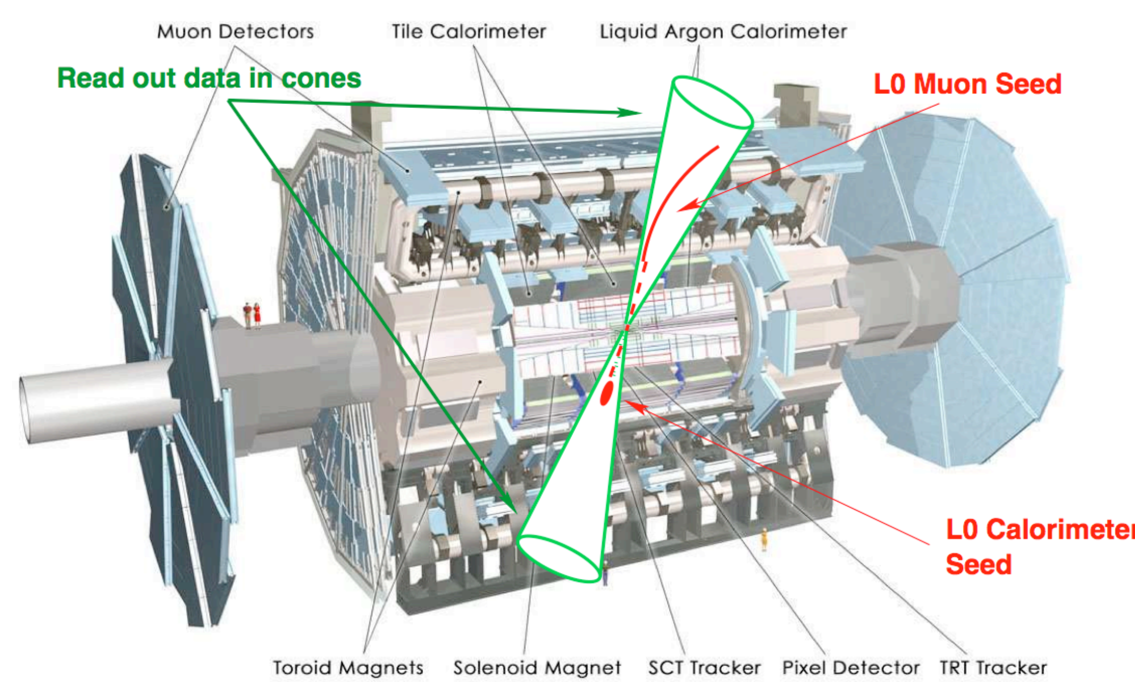


JHEP 08 (2011) 086

Trigger architectures

- PUSH path (CMS)
  - Reduced Tracker information readout at 40 MHz and then combined with calorimeter & muon at L1
    - Trigger objects made from tracking, calorimeter & muon inside a Global Trigger module
- PULL path (ATLAS)
  - Use calorimeter & muon detectors to produce a "Level-0" to request tracking information in specific regions
    - Tracker sends out information from regions of interest to form a new combined L1 trigger



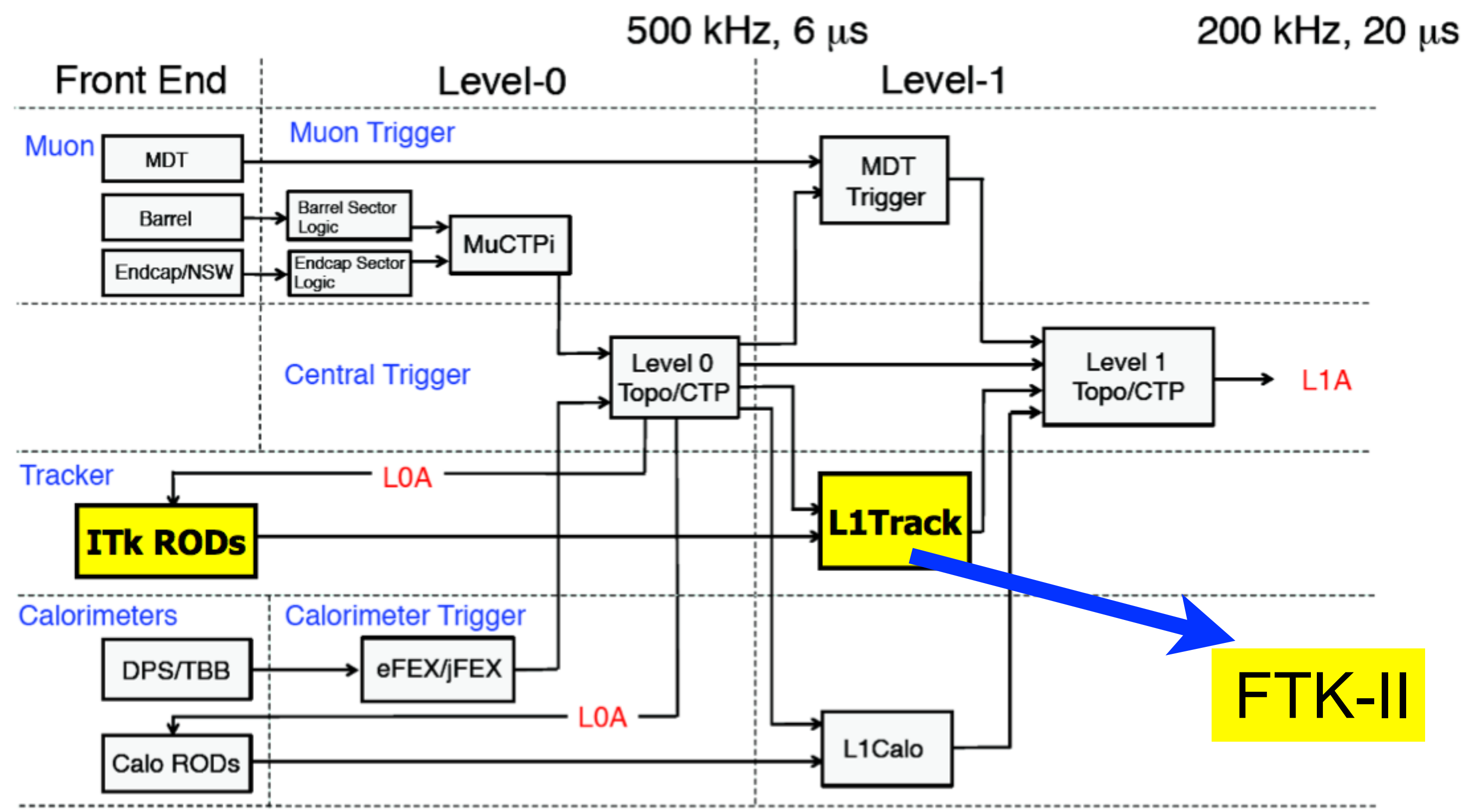


Data reduction

Track Trigger with pull architecture (ATLAS)

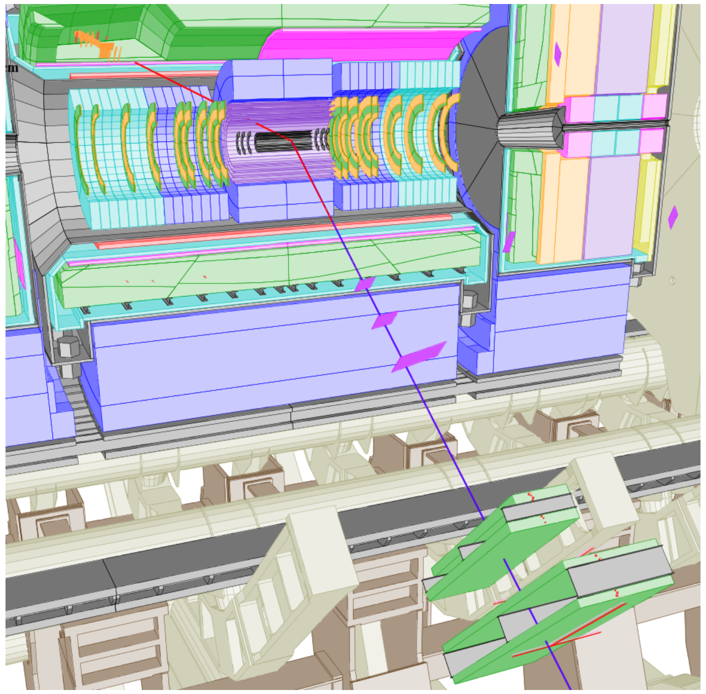
The L0+L1 scheme

- Level-0:
  - Coarse calo and muon data
  - Rate 40 MHz →500 kHz
  - Latency < 6.4 μs
  - Defines Region of Interest (ROIs) for L1
- Level-1:
  - Tracker data only from ROIs
  - Refined information from calo and muons
  - Rate 500 kHz →200 kHz
  - Latency < 20 μs



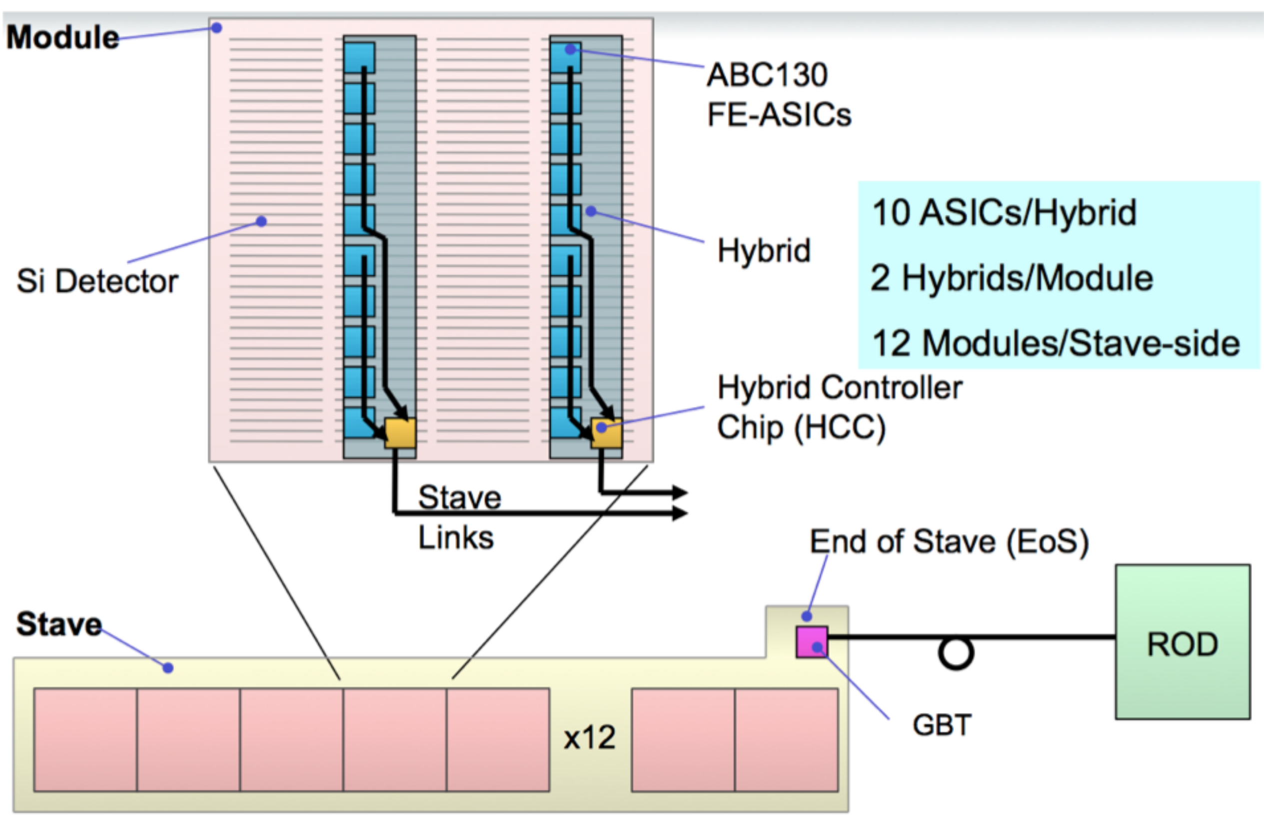
Issues for FTK to be used in Phase 2

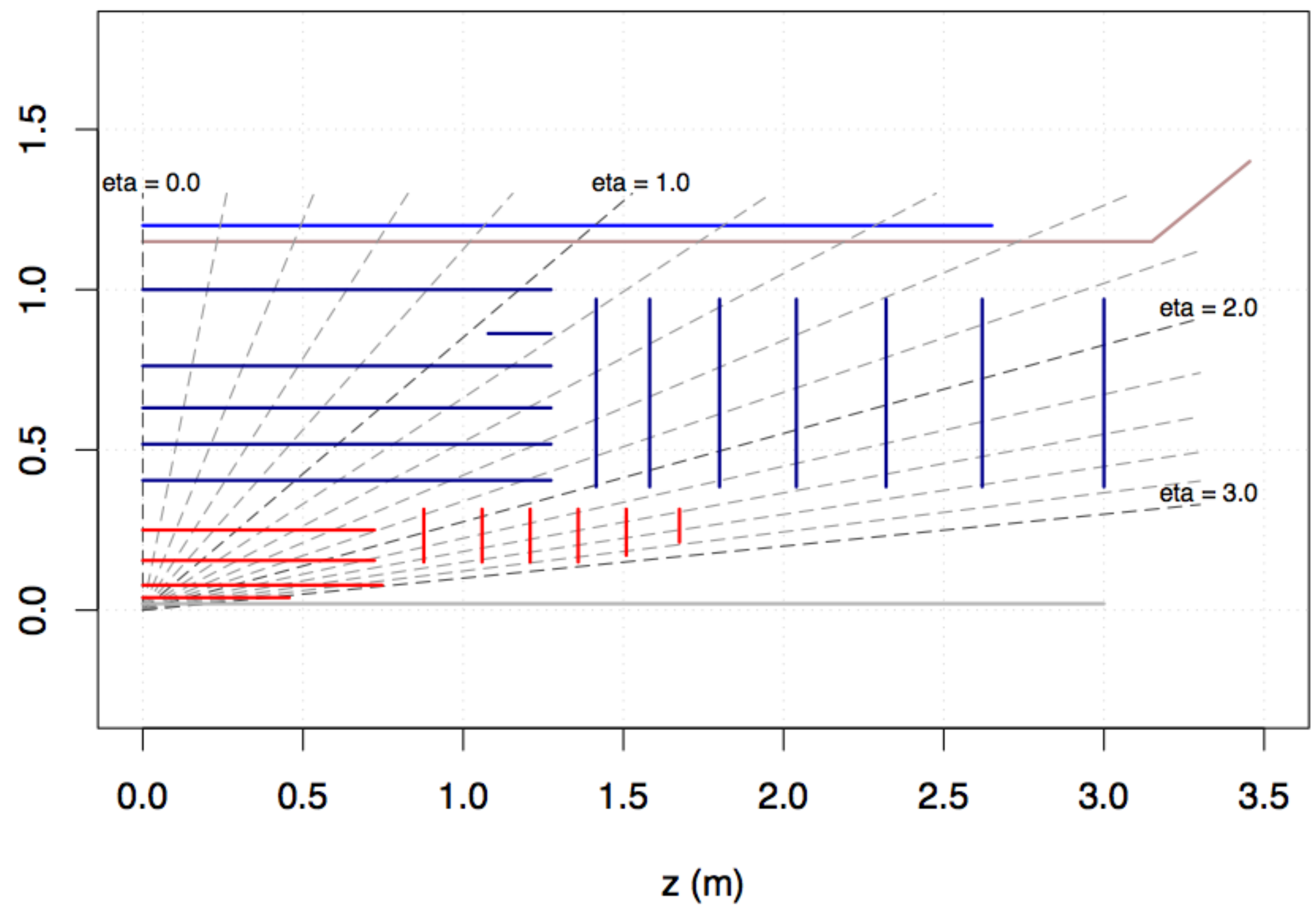
- the larger pileup (x2.5), rate (x5) and granularity
  - increase in the number of patterns by ~one order of magnitude
    - no p_T filtering - rise p_T threshold
- need to cope with shorter latency (20 μs instead of 200 μs)

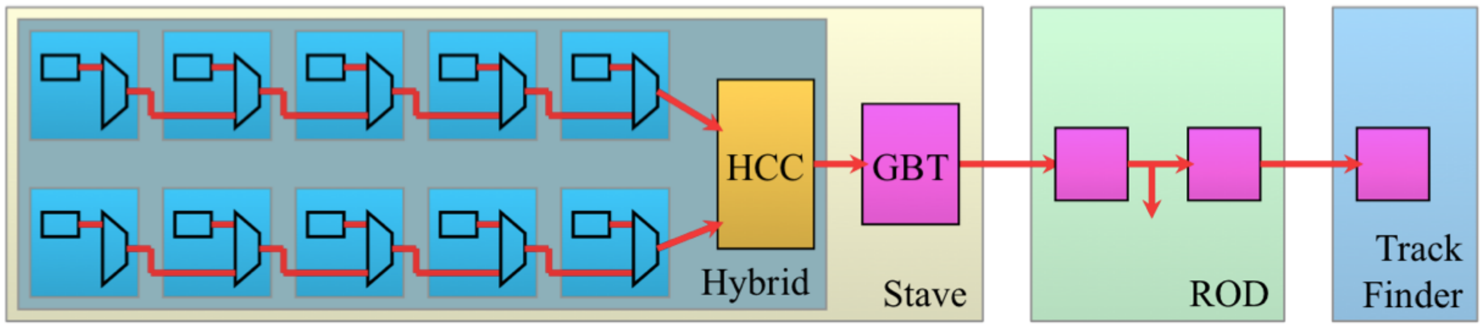


ATLAS readout

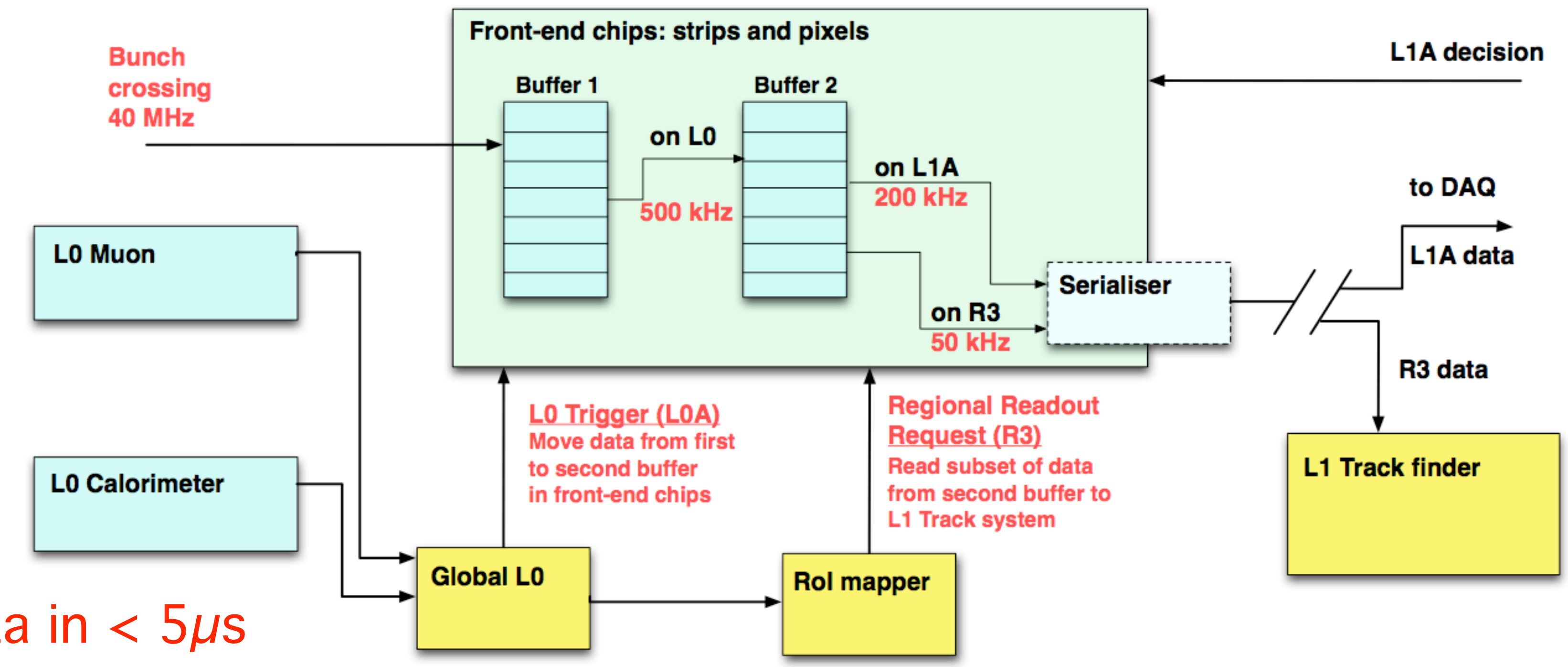
ATLAS Tracker for HL-LHC



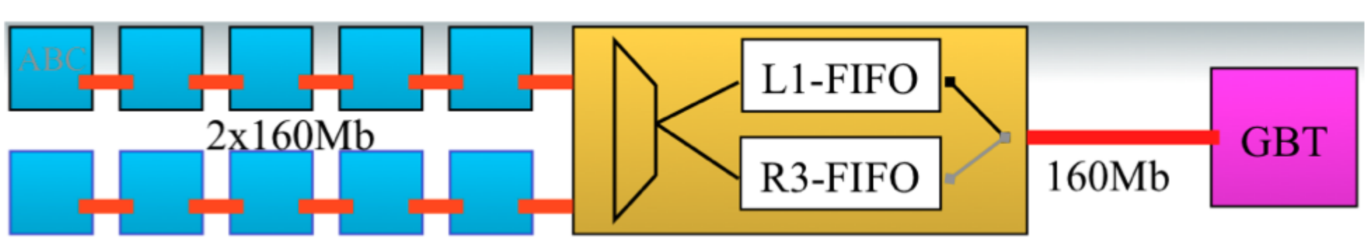


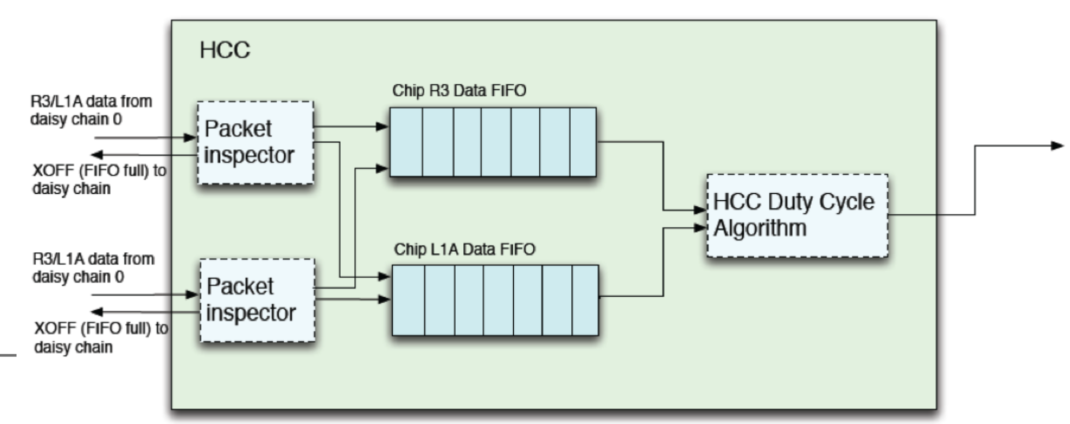


ATLAS L0 and Regional Readout Requests (R3) implementations



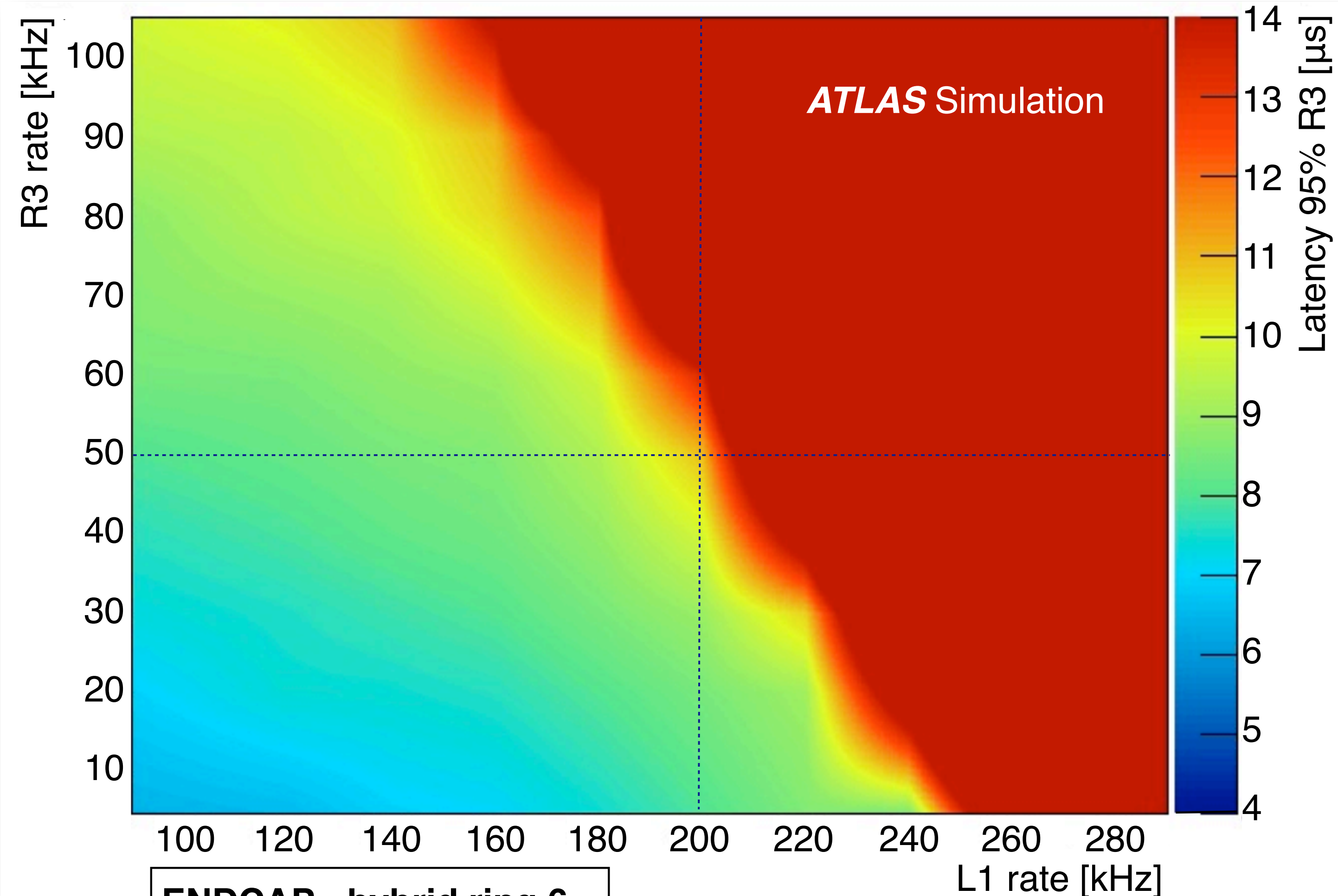
- Trigger data in $< 5\mu s$
  - L0 Trigger accept rate 500 kHz
    - On a L0 accept, copy data from primary to secondary buffer
    - Identify "region of interest" (1-10% of the detector on each L0 accept)
    - Generate a "Regional Regional Request" (R3)
      - Reading only ~10% of the Tracker data, the total bandwidth is only 50% more with the Track Trigger than without.
    - To reduce the latency, a prioritization scheme is envisaged, by using a dedicated R3 buffer





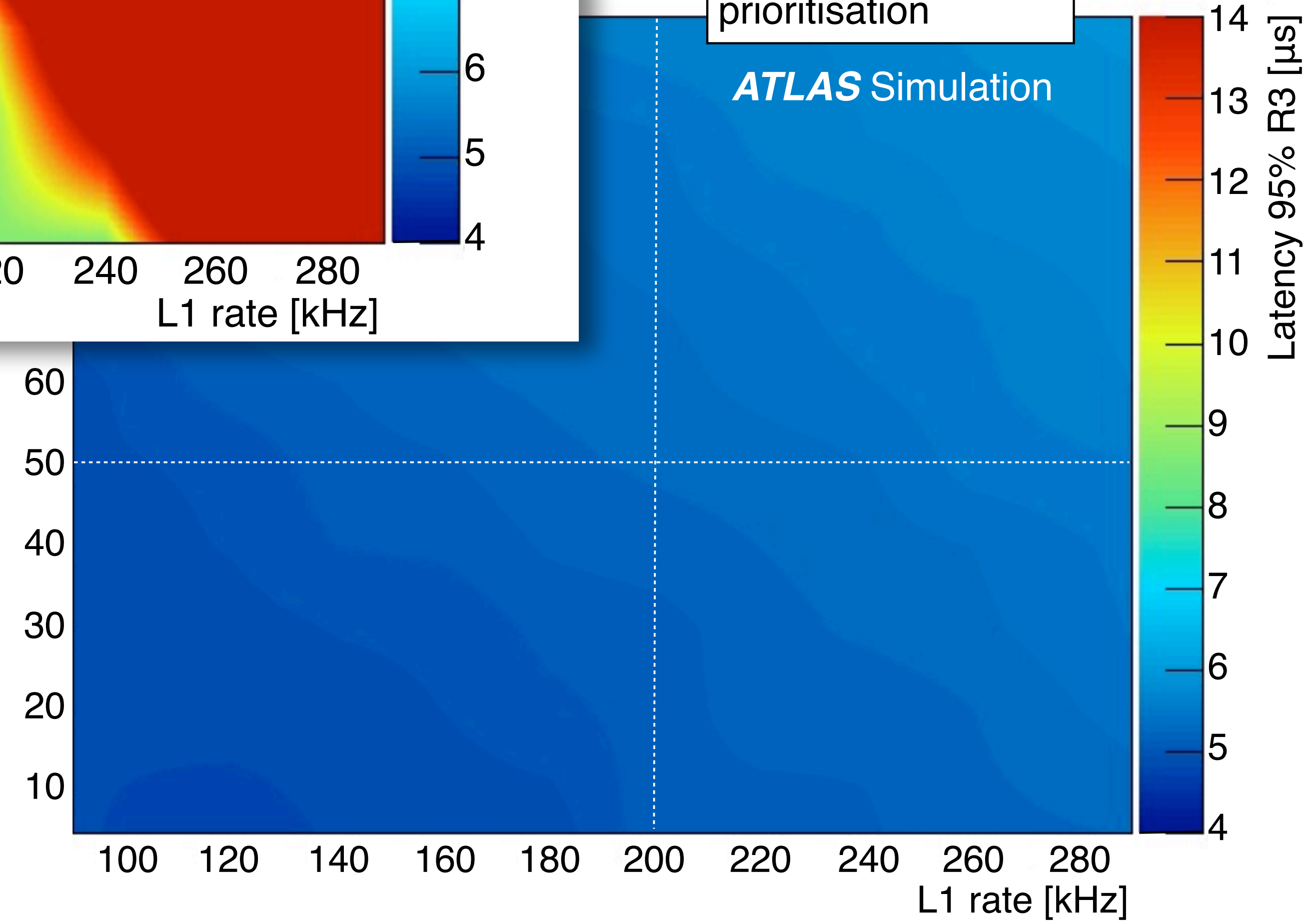
Simulation results - ATLAS

Latency maps



ENDCAP - hybrid ring 6
including R3 HCC
prioritisation

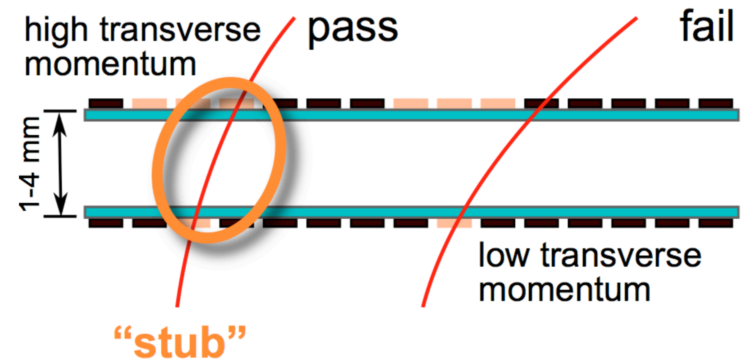
BARREL - layer 0
including R3 HCC
prioritisation

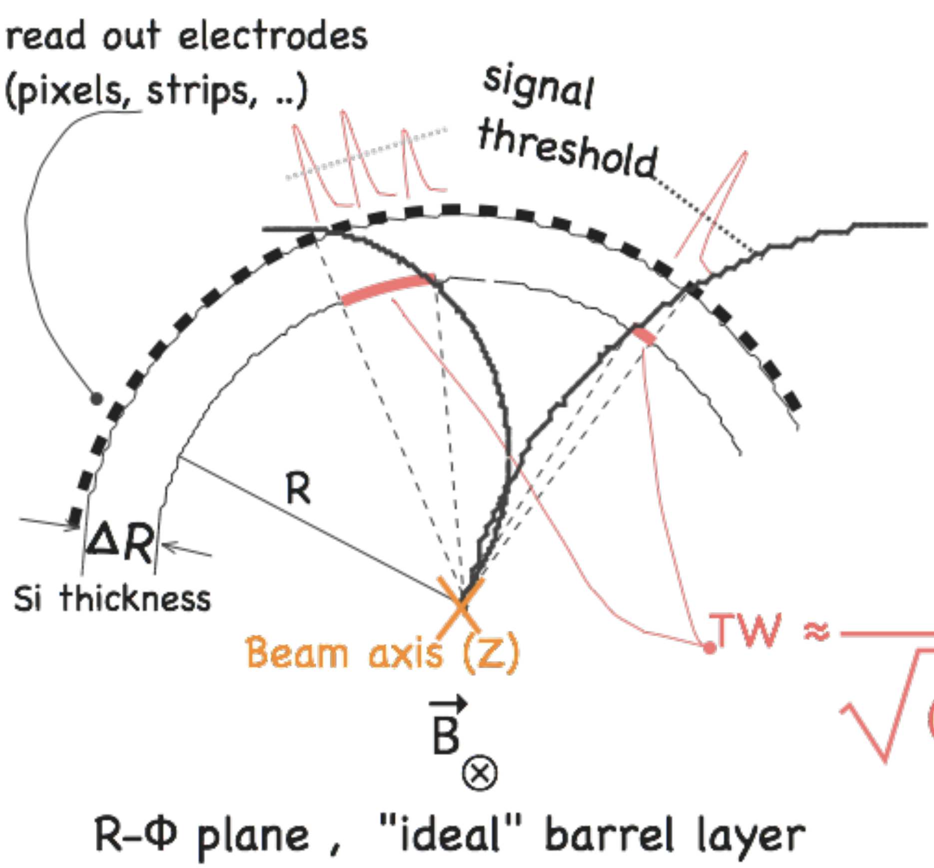


- Barrel acceptable latency over the full phase space when using prioritisation on the HCC
- Endcap hybrids run 4, 5 and 6 have an issue due to limited HCC bandwidth and chip multiplicity

Select only hits from “high-p_T” tracks

- Select “high-p_T” tracks (>2 GeV) by correlating hits in 2 nearby sensors (stub)





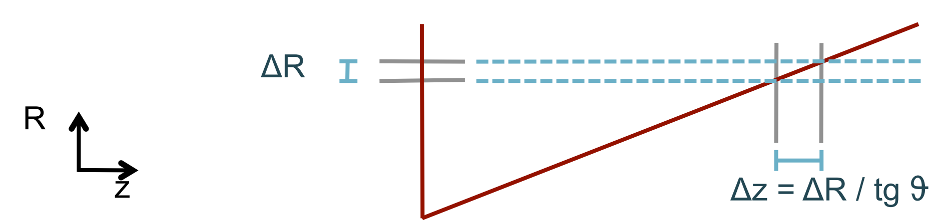
$$TW \approx \frac{\Delta R}{\sqrt{\left(\frac{pT}{pT_{min}}\right)^2 - 1}} \approx \Delta R \frac{pT_{min}}{pT} = 0.15\, B\, \Delta R \frac{R}{pT}$$

F. Palla, G. Parrini, PoS VERTEX2007 (2007) 034, http://pos.sissa.it/archive/conferences/057/034/Vertex%202007_034.pdf

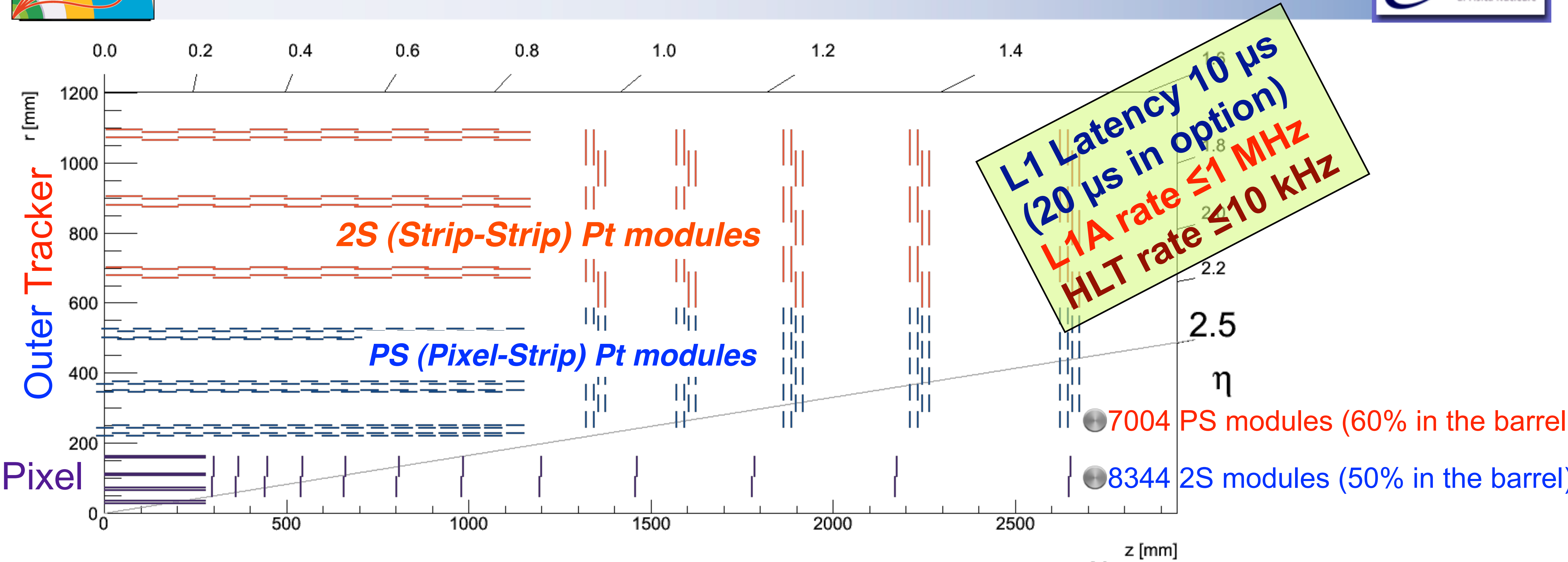
J. Jones, A. Rose, C. Foudas, G. Hall, http://arxiv.org/pdf/physics/0510228v1.pdf

Large B field of CMS beneficial!

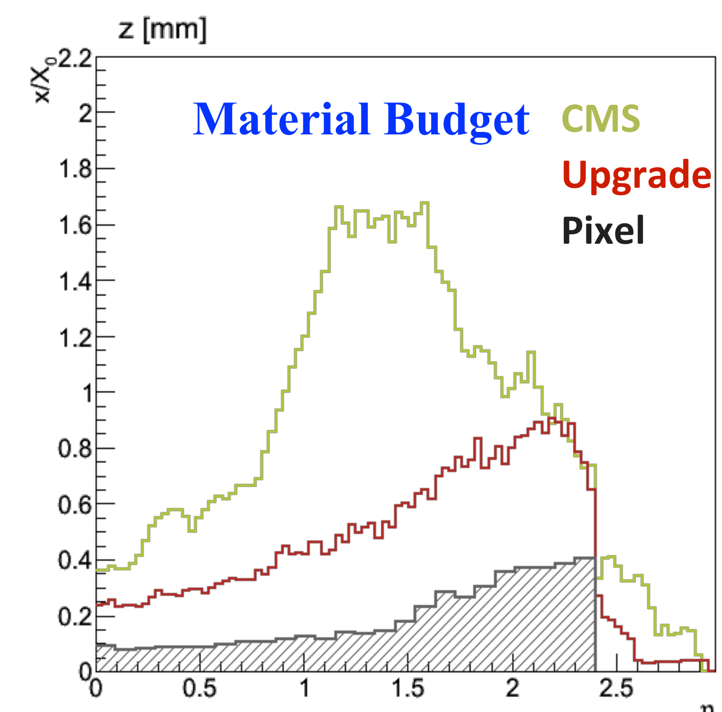
- In the barrel, ΔR is given directly by the sensors spacing
- In the end-cap, it depends on the location of the detector
  - ➡ End-cap configuration typically requires wider spacing (up to ~ 4 mm)



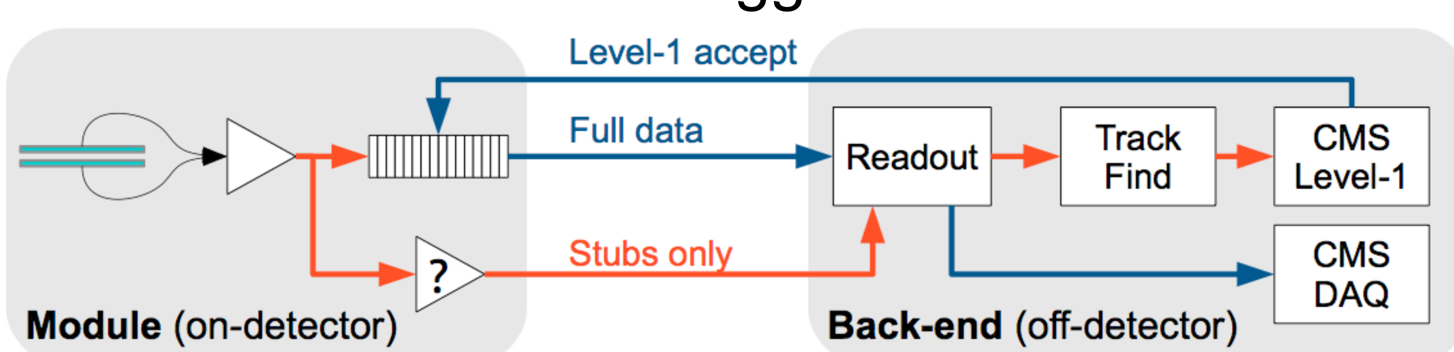
CMS Upgraded Tracker



Better p_T resolution and lighter than current tracker

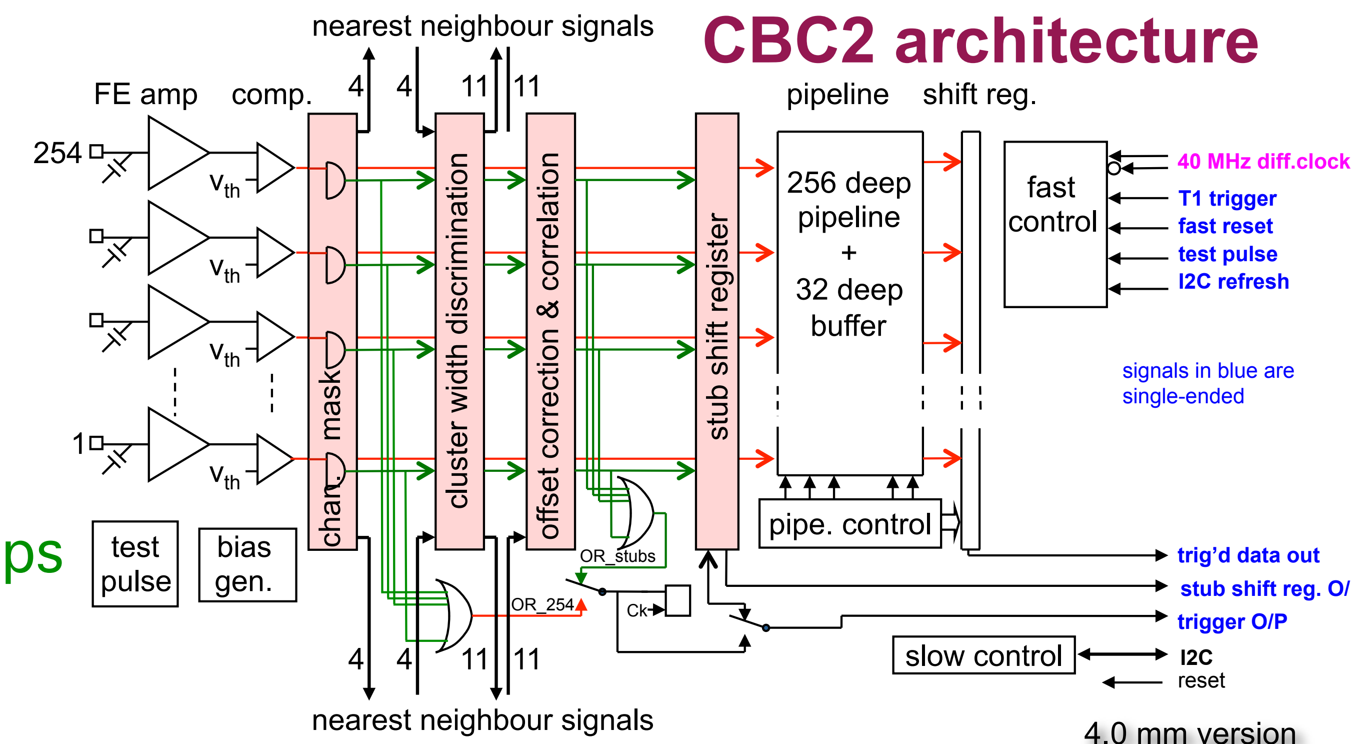


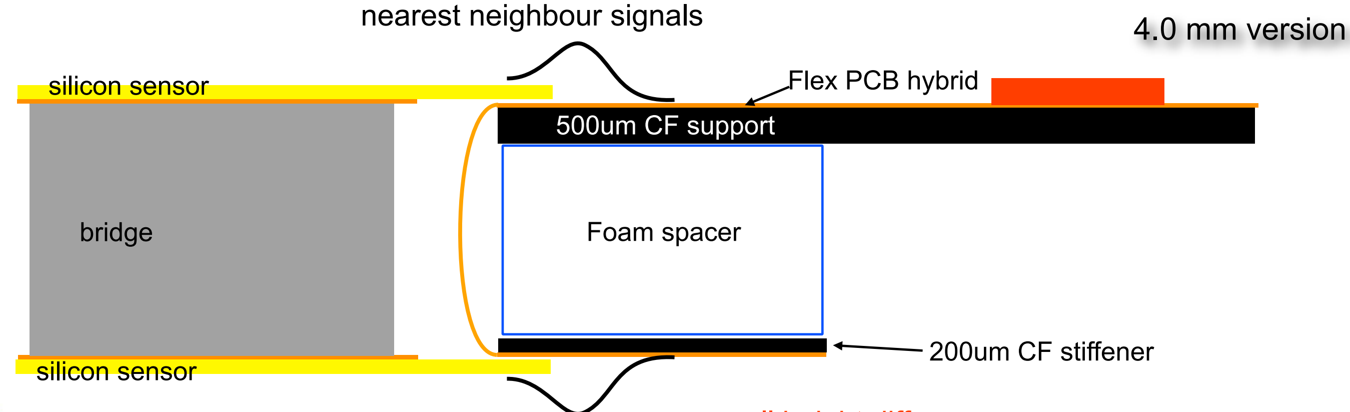
Readout and Trigger schematics



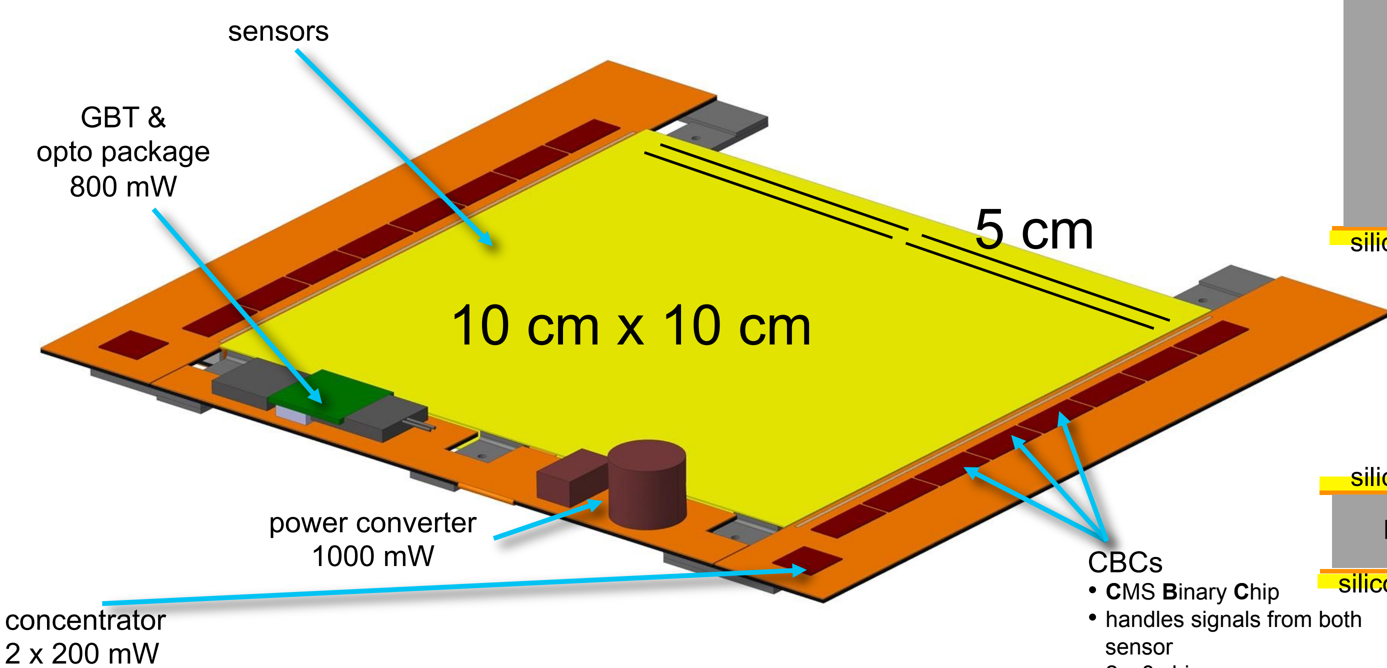
2S(trip) sensors modules

- 100 μm x 5 cm long strips on both sensors
- readout by 8 CBC on either sides
  - First discriminates signals by rejecting large clusters; then form a coincidence between the two sensor planes
  - Concentrator chip sends data from 8 chips to GBT

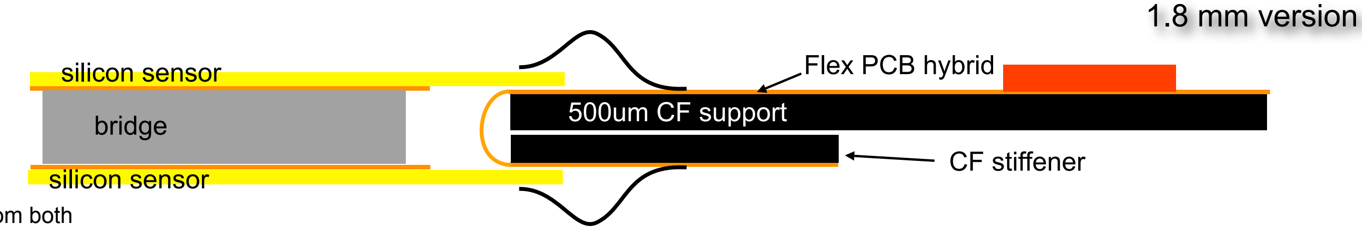




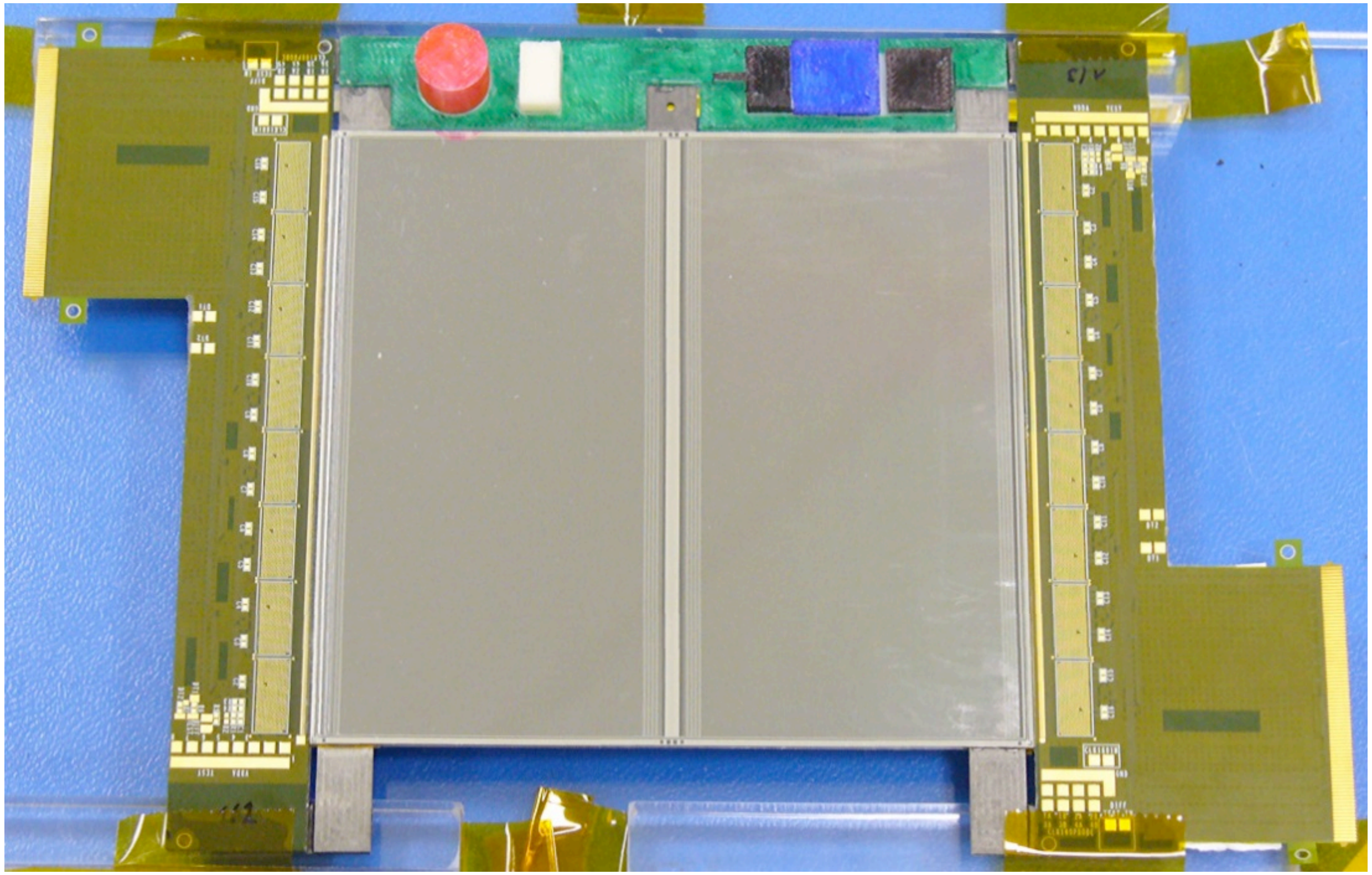
- small height difference
- short wires (<3 mm)
- encapsulation of bond wires possible

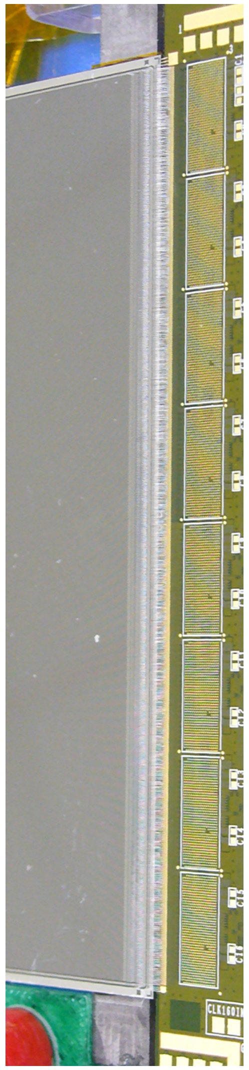


CBCs
- **C**MS **B**inary **C**hip
- handles signals from both sensor
- 2 x 8 chips
- 1200 mW

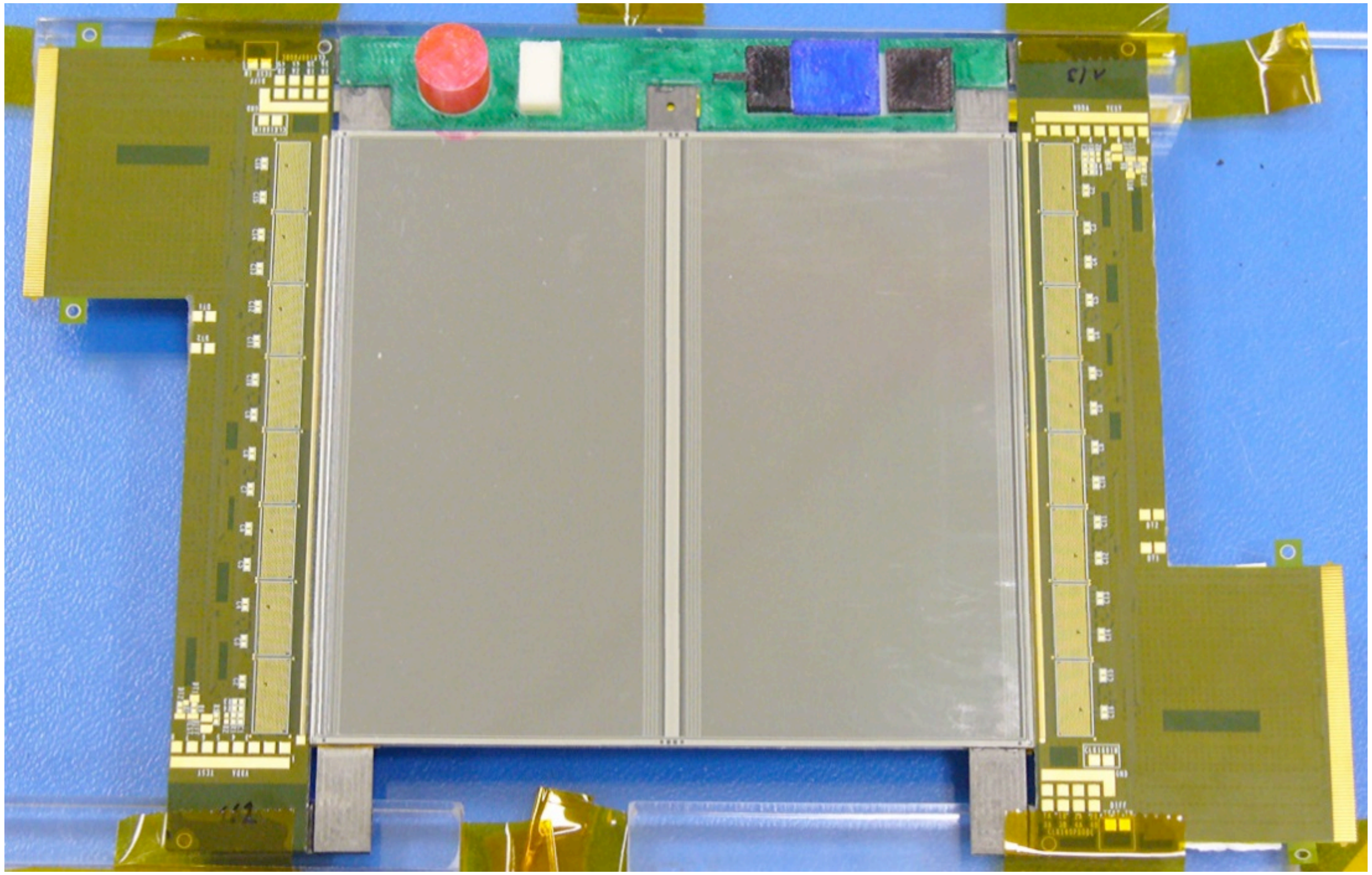


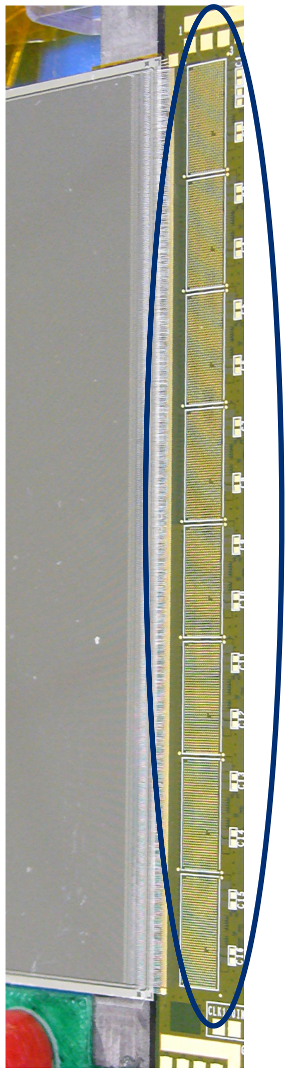
2S module prototype



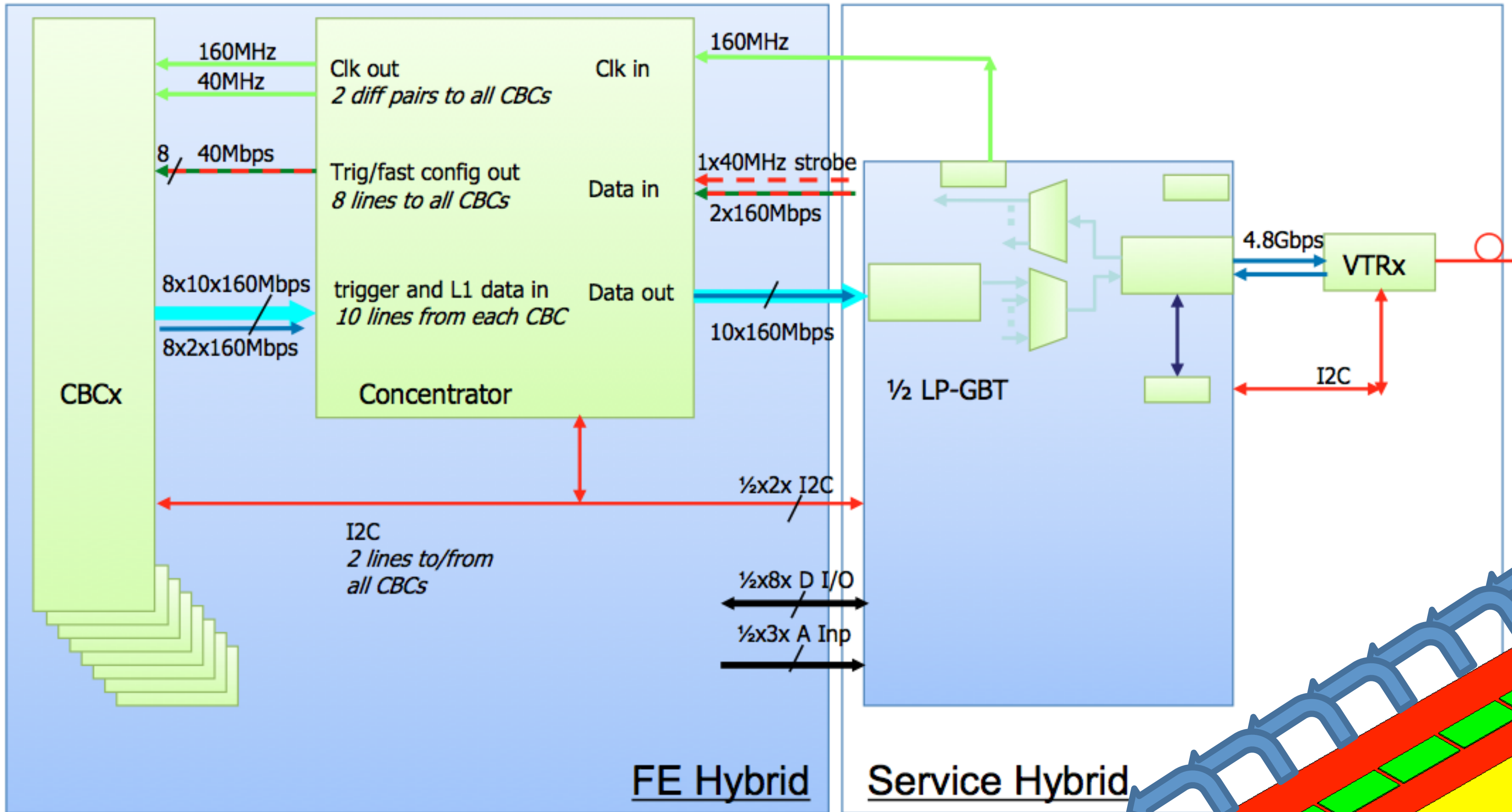


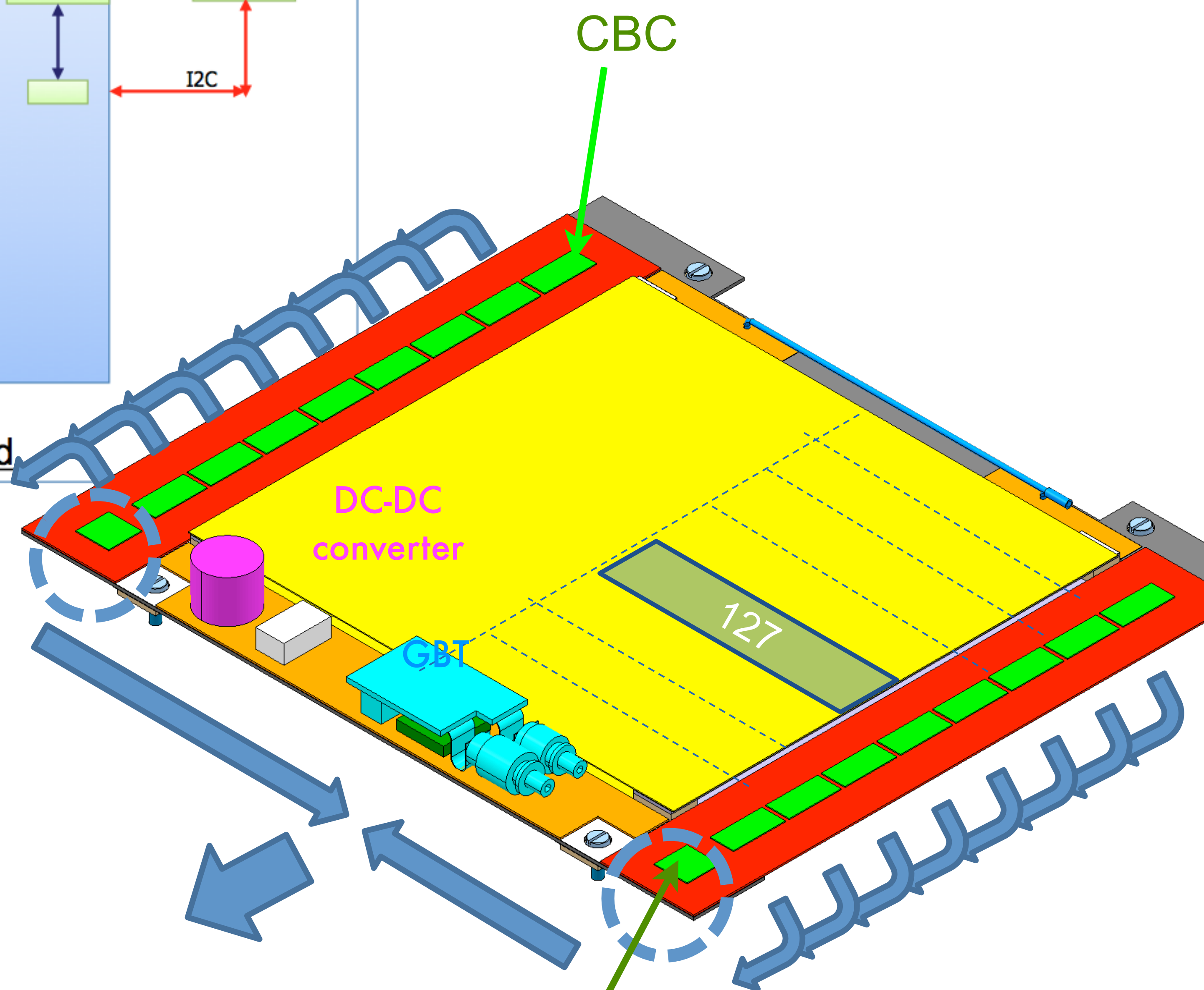
2S module prototype





1016 strip bond wires



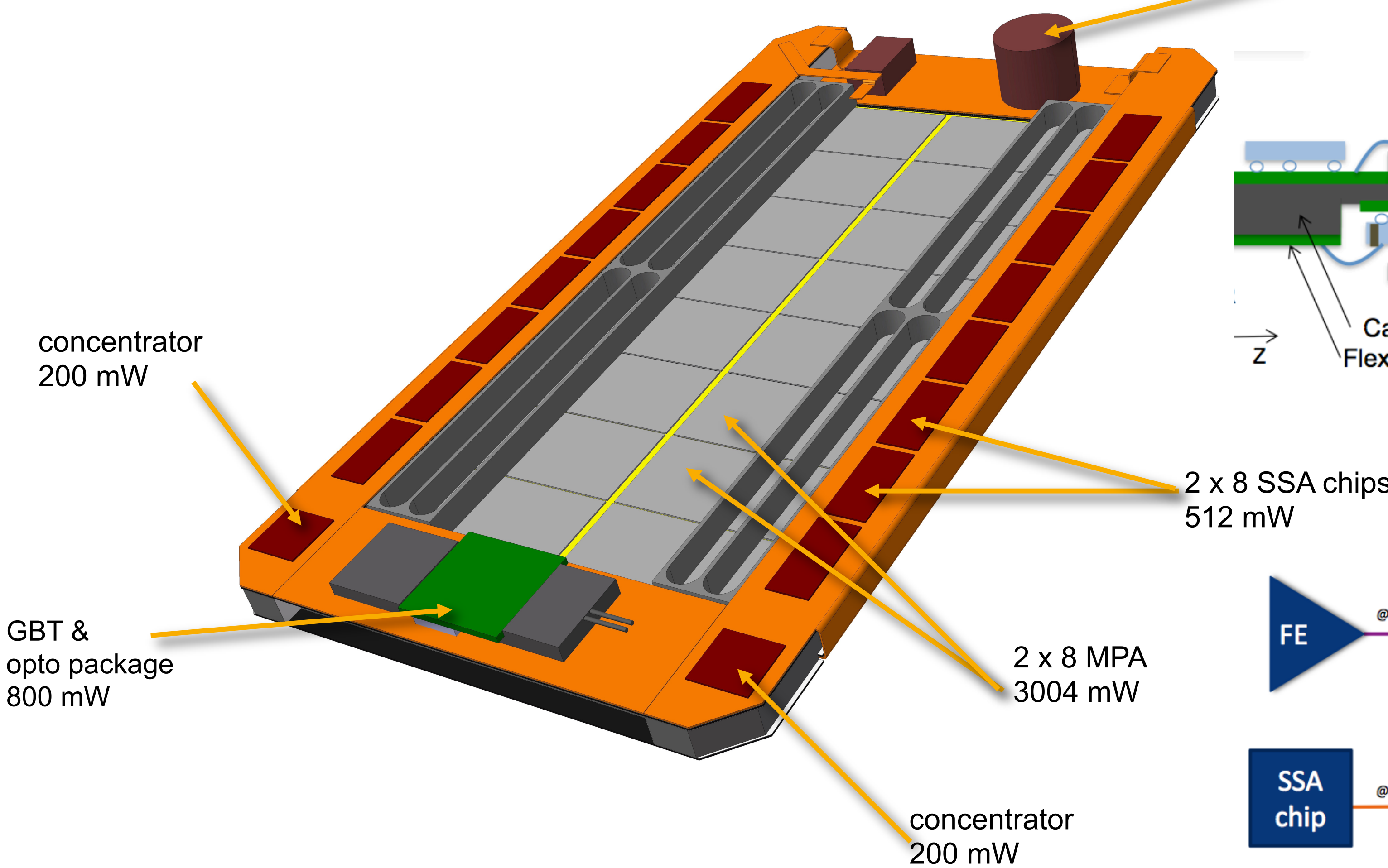


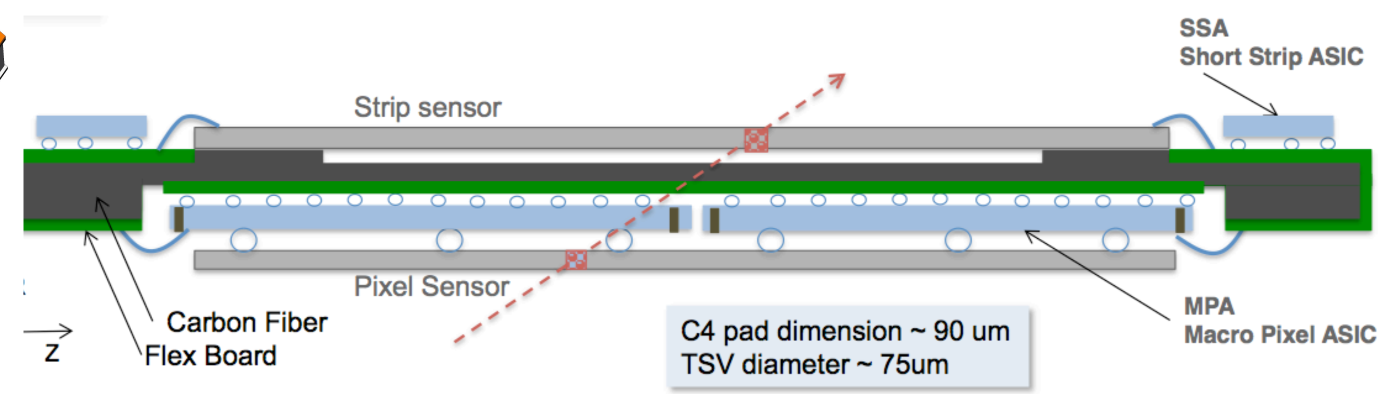
CBC outputs up to 3 stubs/bx, 160 MHz x 10 bits

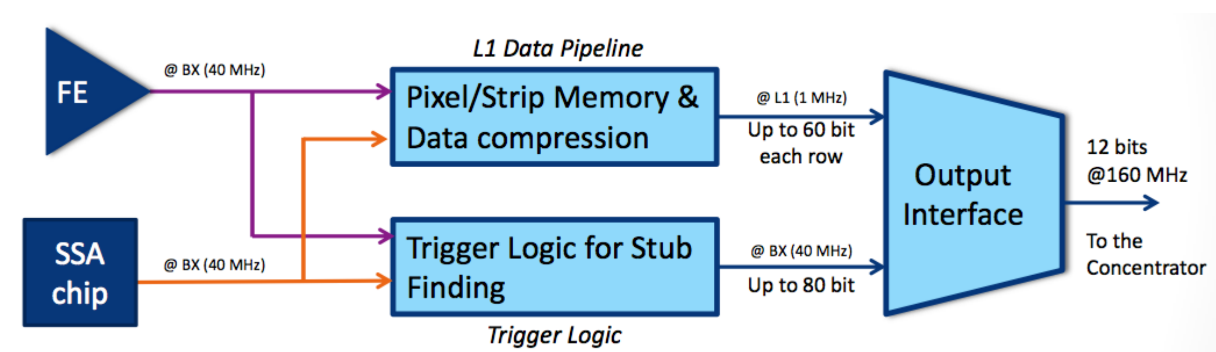
Concentrator chip receives 8 CBC and sends out up to 12 stubs/8bx, 160 MHz

P(ixel)S(strip) module

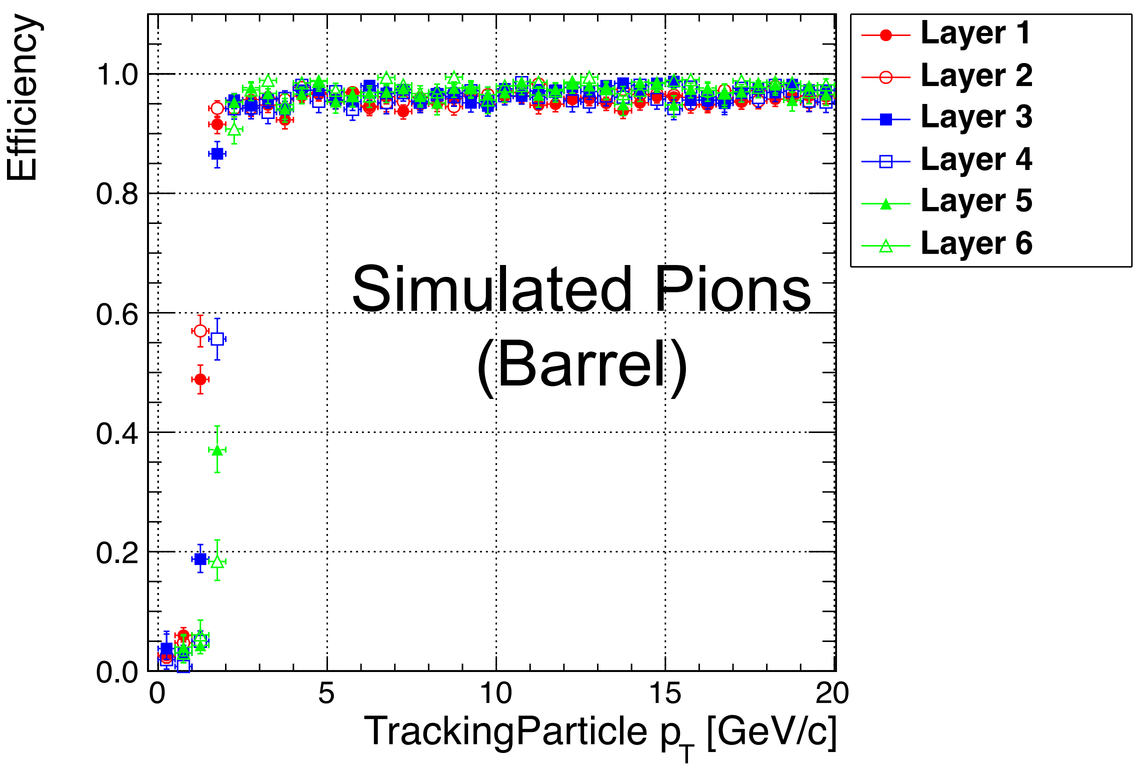
- strips = 100 μm x 2.4 cm
- pixels = 100 μm x 1.5 mm
  - Pixels are logically OR-ed for finding coincidence in the r-φ plane, and the precise z-coordinate is retained in the pixel storage and provided to the trigger processors.

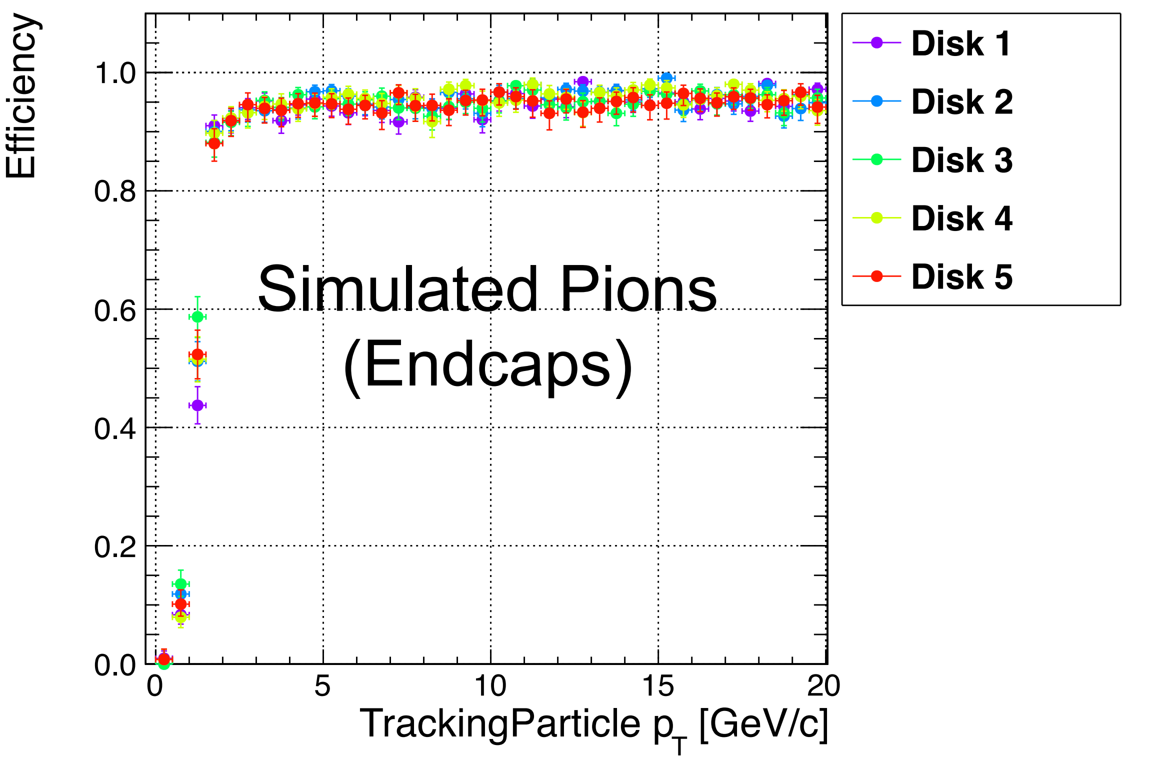




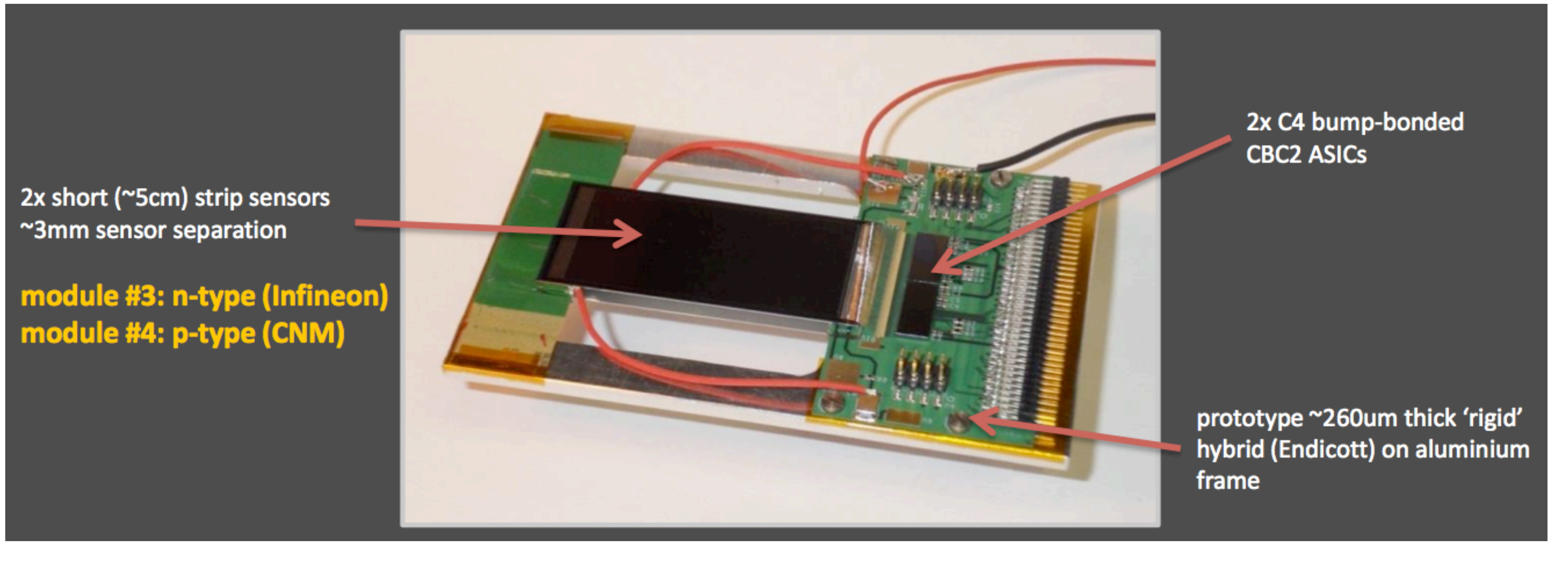


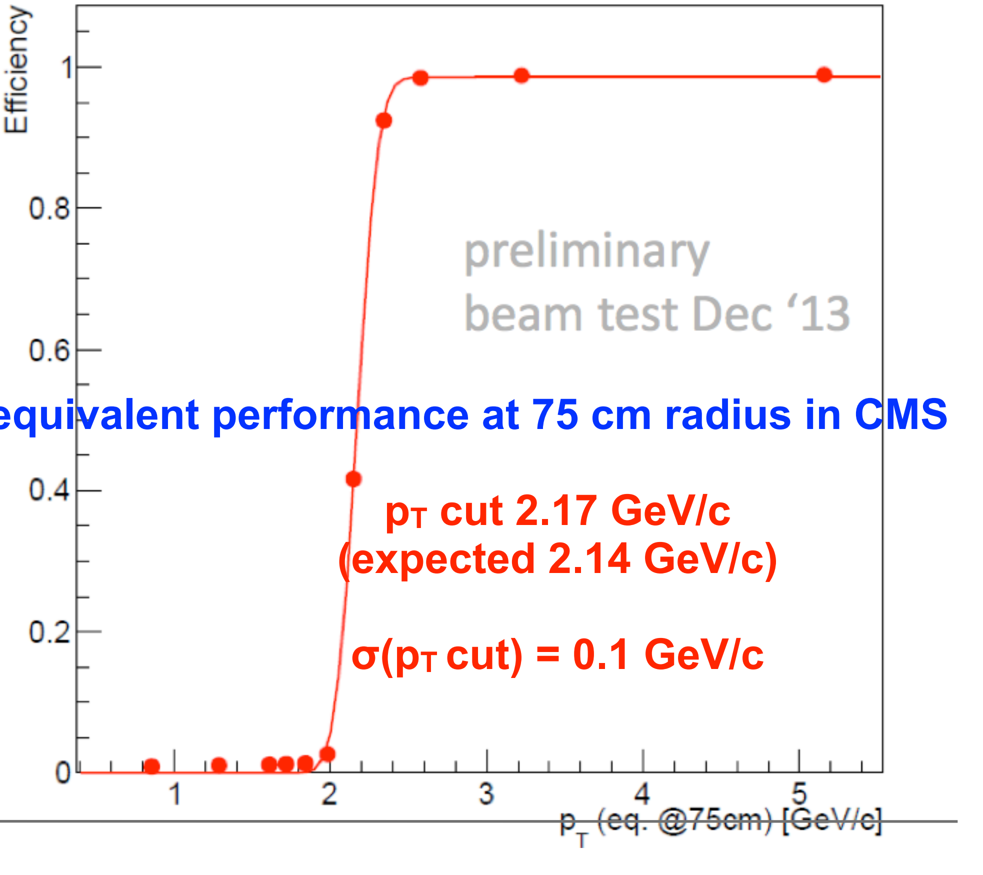
p_T modules performances





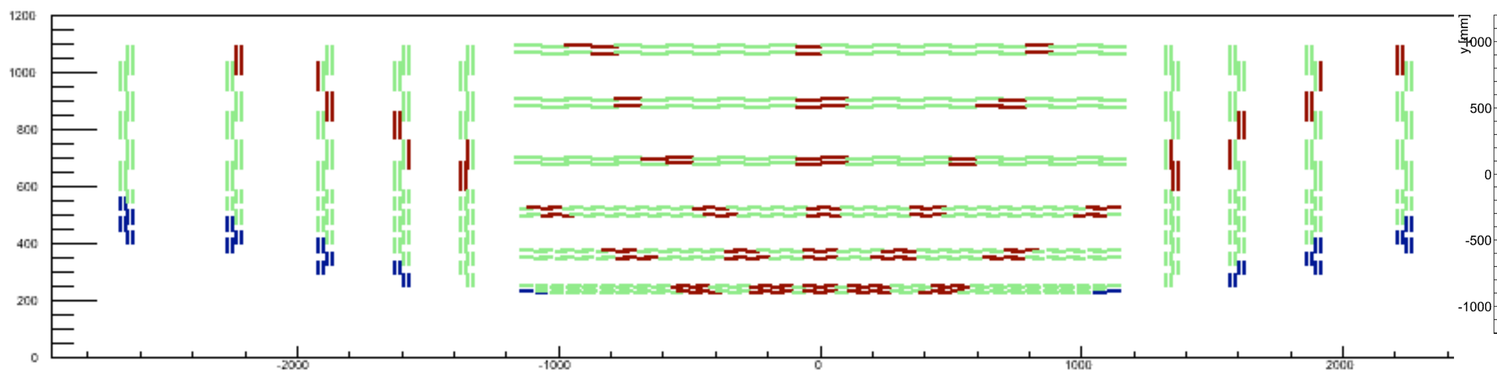
Prototype module test beam at DESY (2-4 GeV e^+)

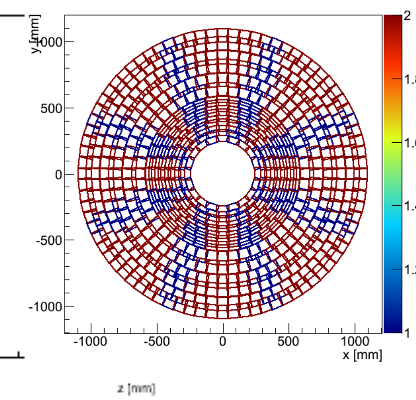


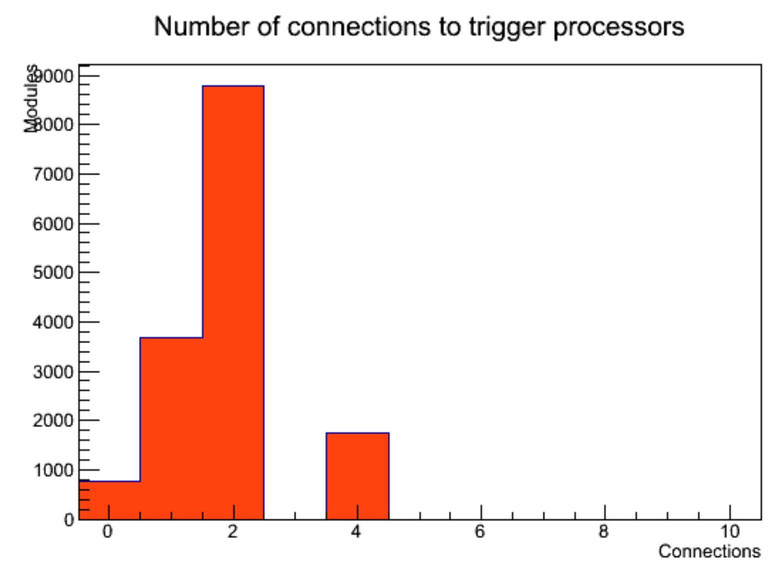


Data organization and dispatch

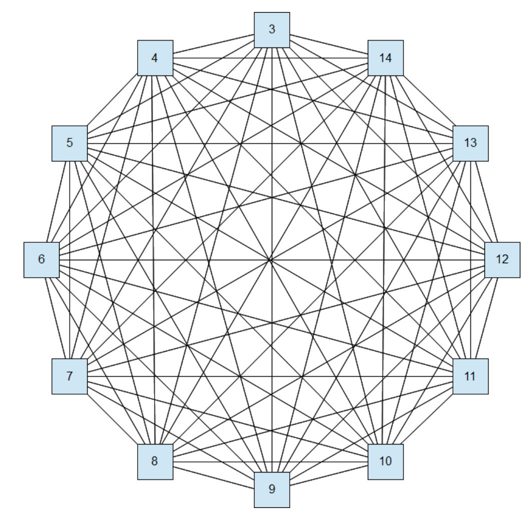
- Subdivide tracker into trigger towers
  - Example CMS: 8(r-ϕ)x6(r-z) trigger sectors (some 10% overlapping)
    - Each sector ~200 stubs on average; tails up to ~500 stubs/event in 140 evts pileup+ttbar (to be compared with ATLAS-Phase 1 ~2000)
      - About 600 Gb/s per one trigger tower







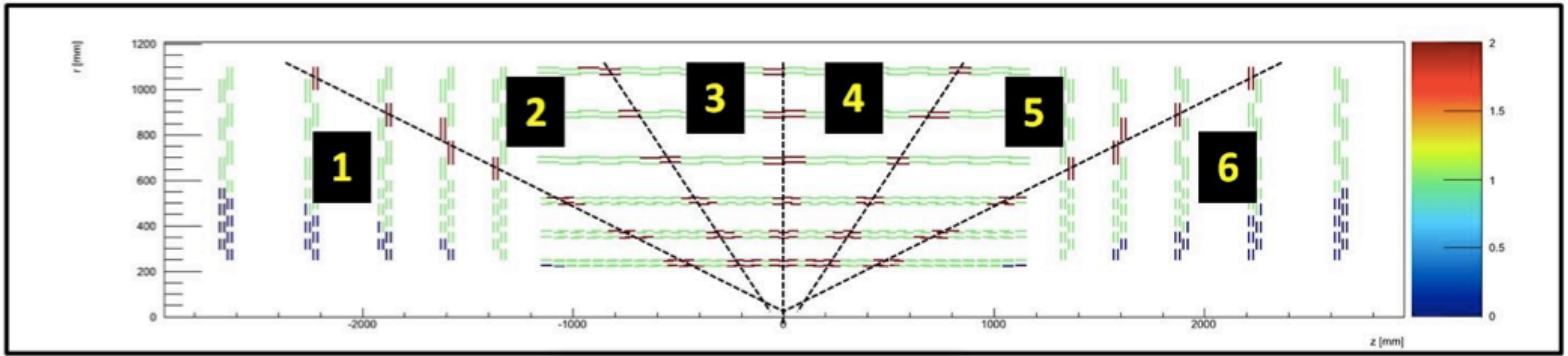
- Send data to Track-finding processors
  - Full mesh ATCA shelfs
    - Capable of “40G” full-mesh backplane on 14 slots = 7.2 Tb/s
    - Several options being investigated, all include time multiplexing data transfer from a set of receiving processors boards to pattern recognition and track finding engines
    - O(10) time multiplexed at the shelf level
    - keep latency < 5 μs, including pattern recognition and track fitting



Trigger Tower segmentation

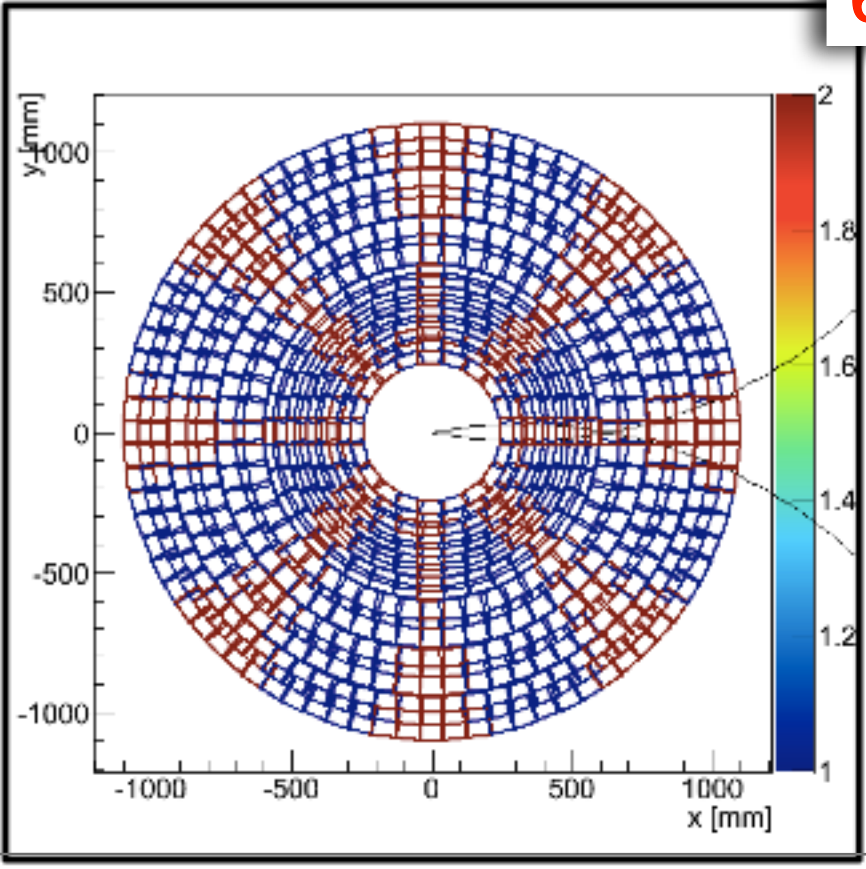
Regional multiplexing => divide the detector into trigger towers

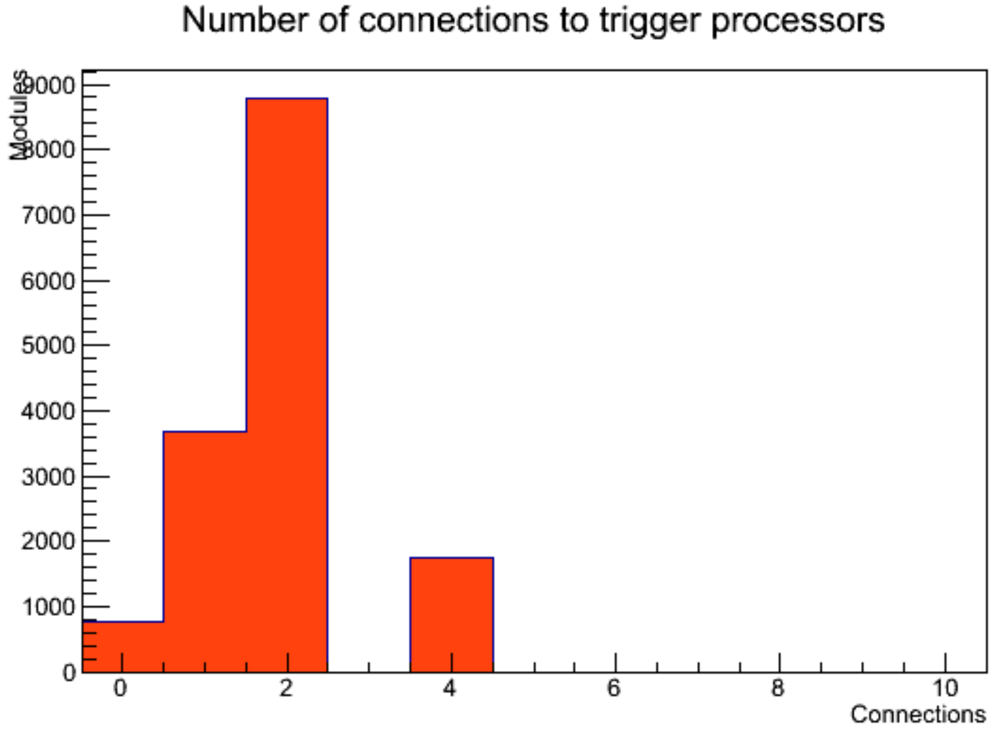
6 regions in η



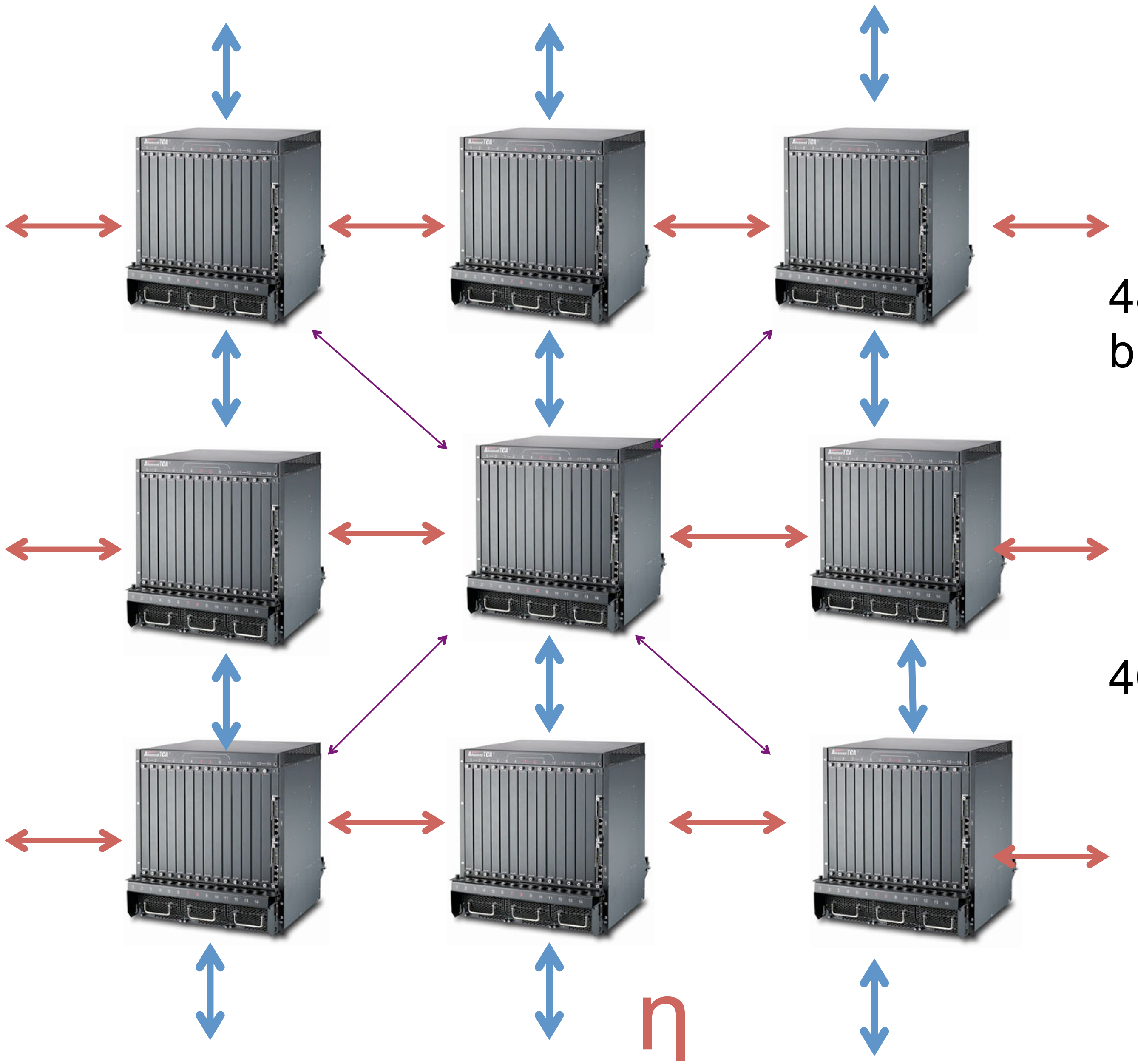
6 (η)x8 (ϕ) regions

8 regions in r-phi





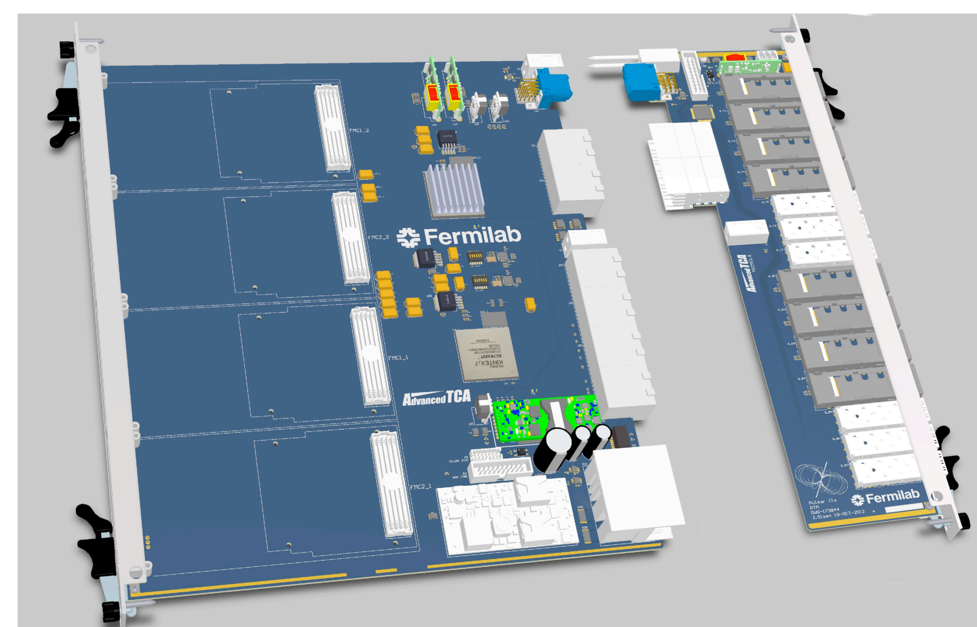
Tower interconnections



48 x 10 Gbps
bidirectional

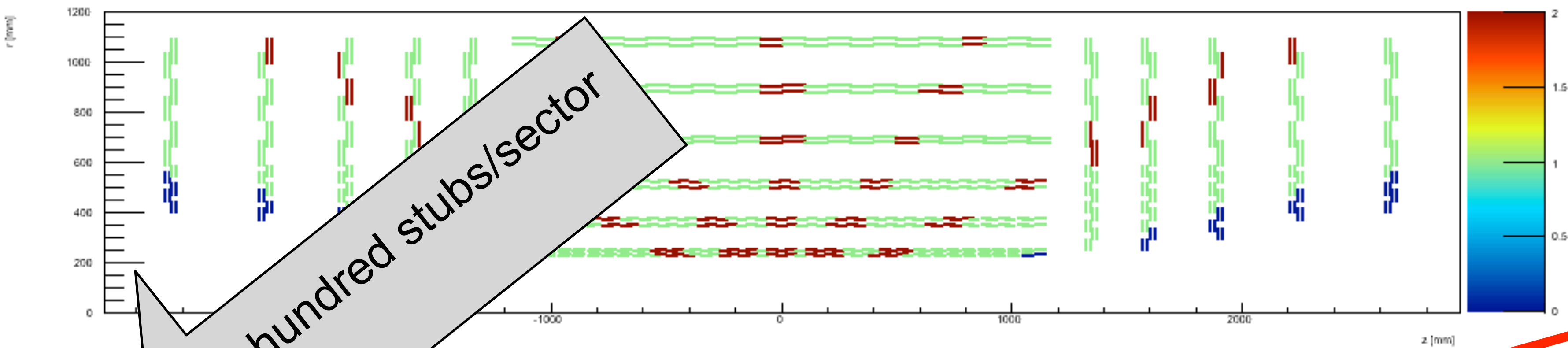
φ

40G full-mesh backplane



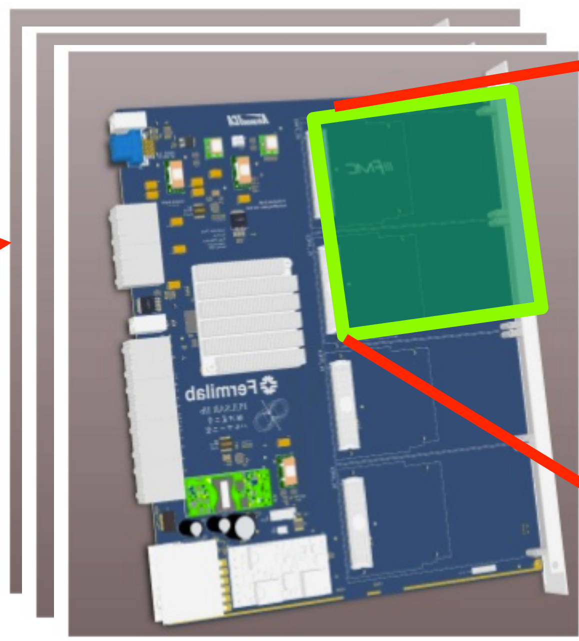
Neighbors
data sharing

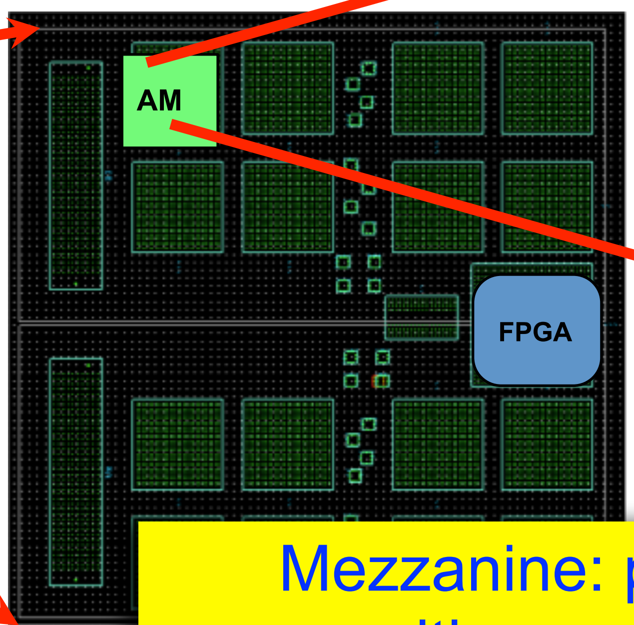
L1 Track finding concept



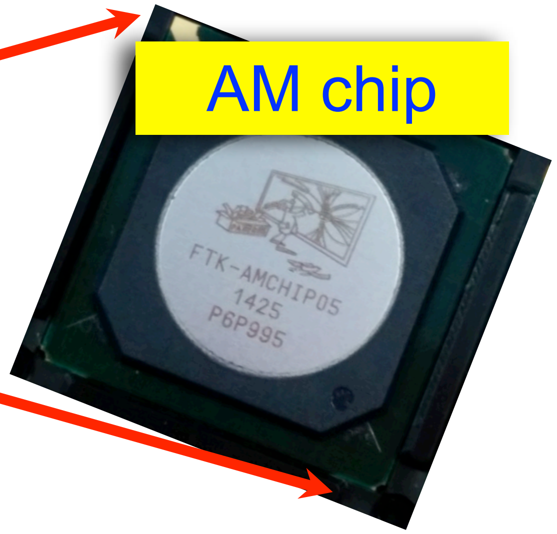
few hundred stubs/sector

40-100 G full mesh ATCA shelf

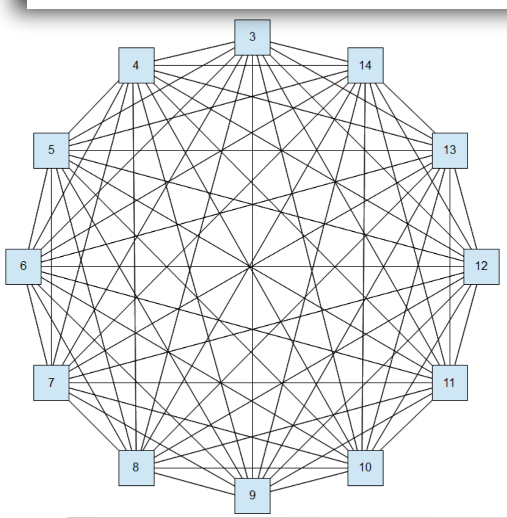




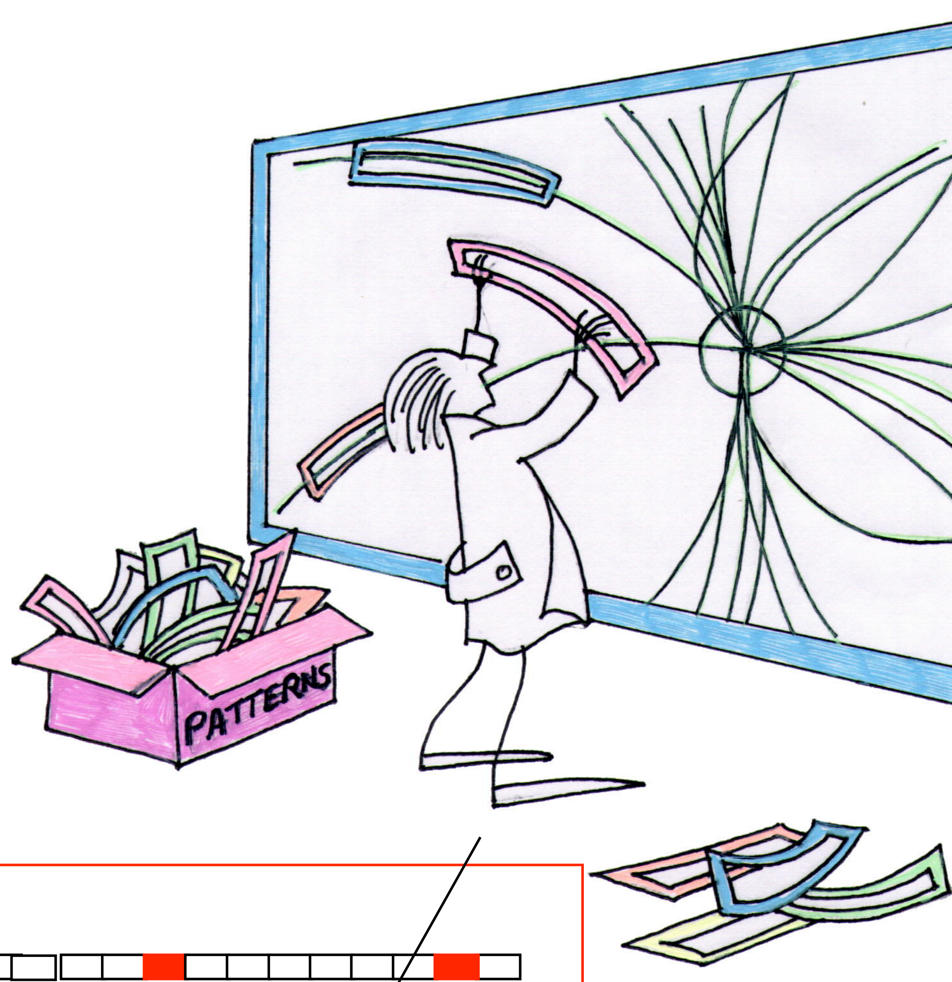
Mezzanine: pattern recognition and track fit



AM chip

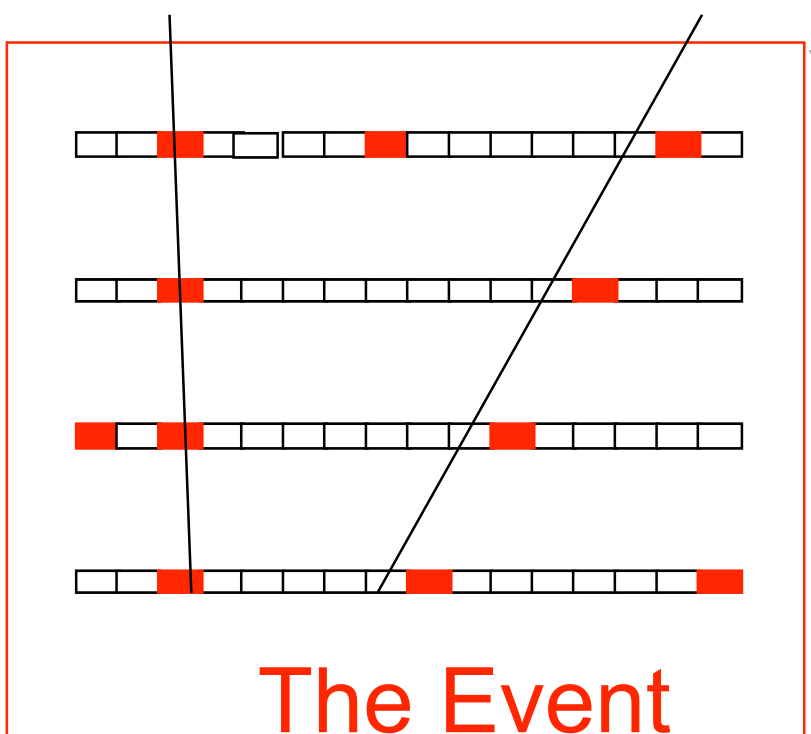


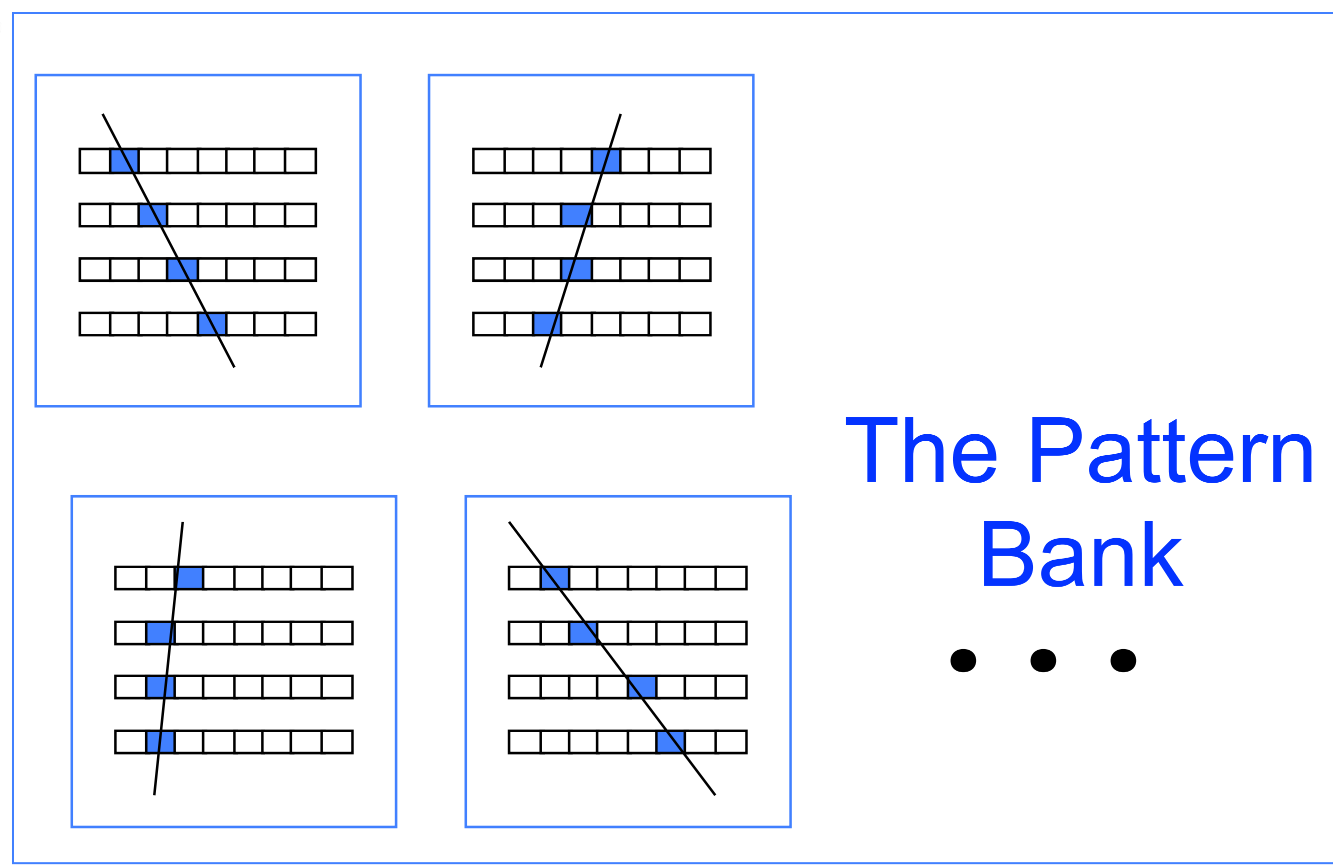
- Send data to PRM in each ATCA shelf
  - Data distributed to Pulsar boards in time multiplexed mode
  - Perform pattern recognition using AM chips
  - Track fit with FPGA (PCA, Hough transform, Retina etc)



The pattern bank is flexible set of pre-calculated patterns:

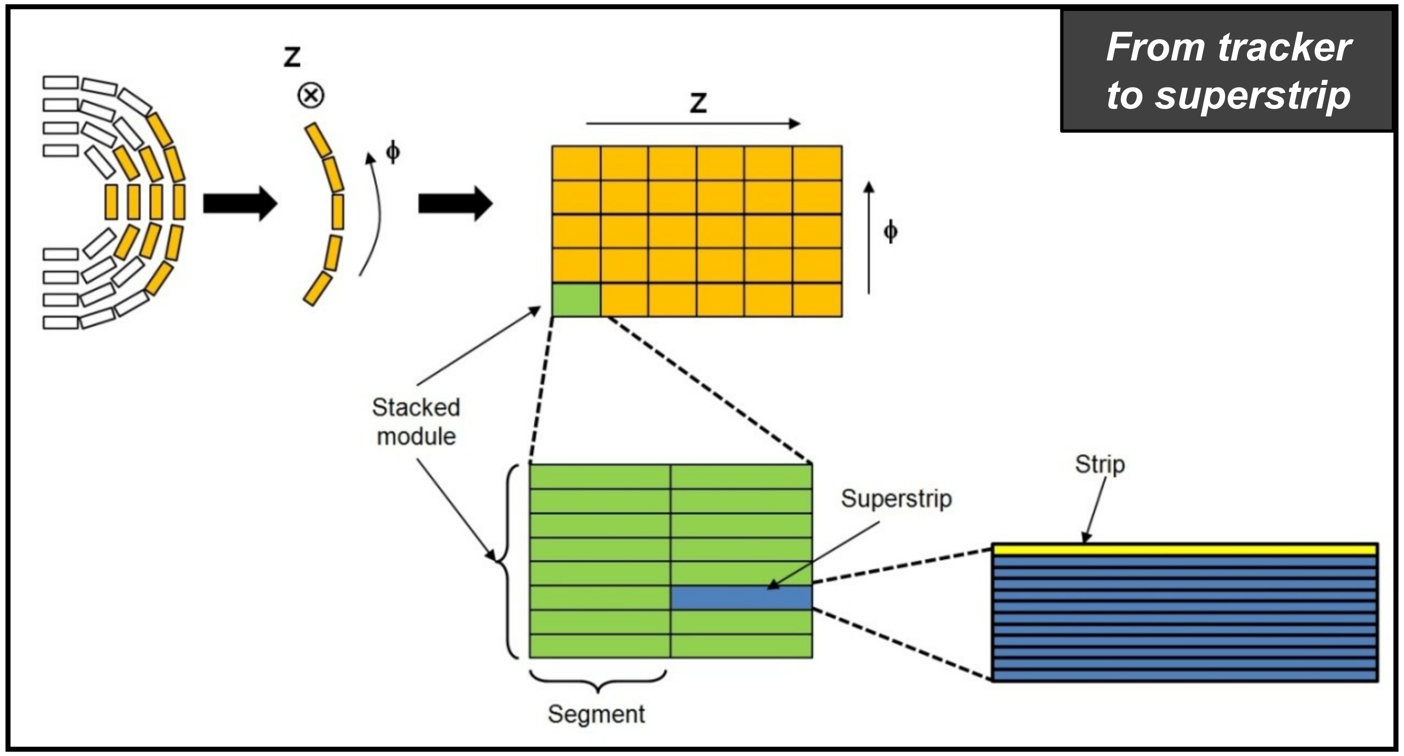
- can account for misalignment
- changing detector conditions
- beam movement
- …





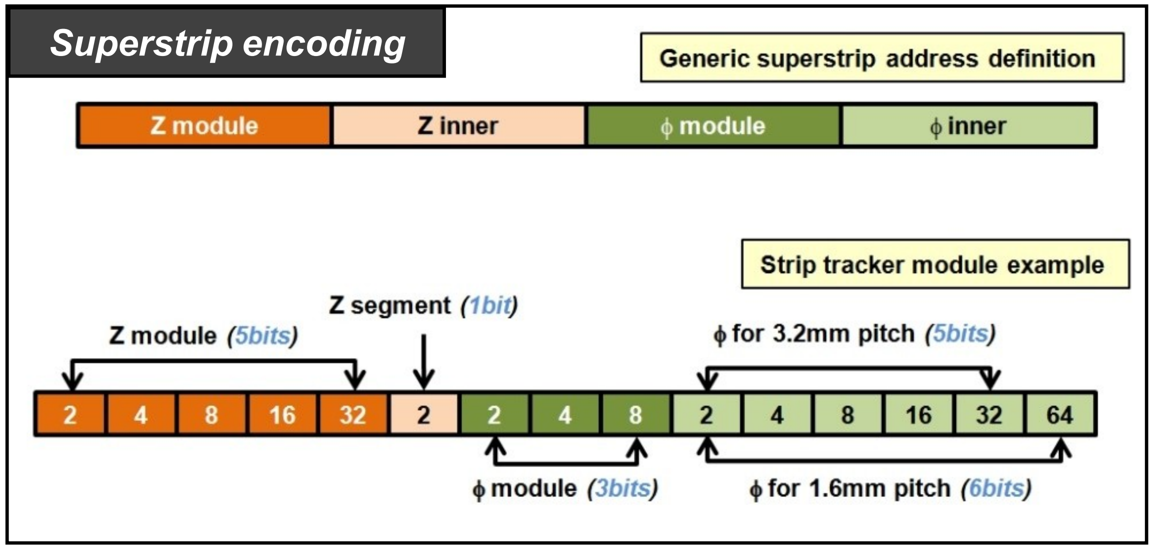
A pattern

→ **Superstrip definition:**



→ **A superstrip is simply a bunch of strips in one module of the tracking detector.**

→ **The superstrip address is the info sent to the AM board. Is is coded on a certain number of bits, depending on the superstrip resolution.**

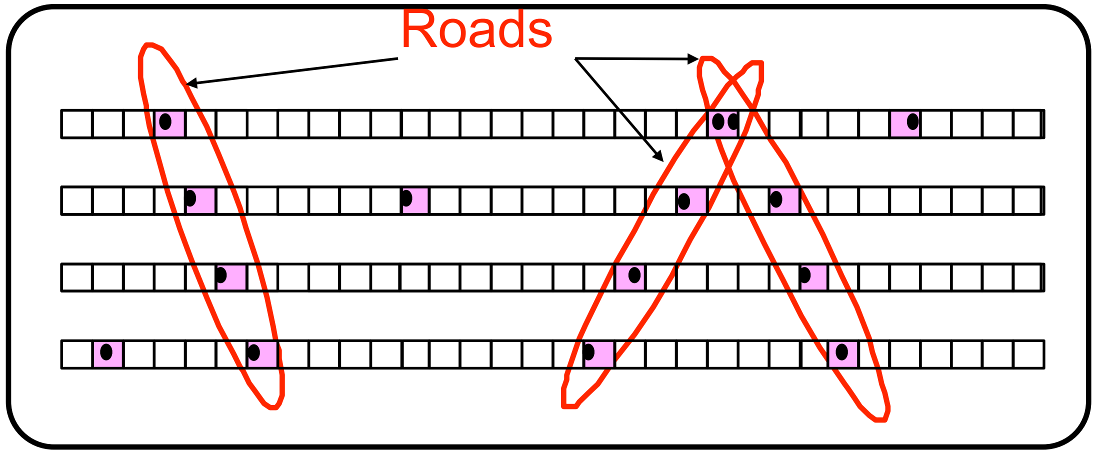


→ **The encoding is divided into 4 parts, giving module and intra-module SS position in Z and ϕ direction (*R is not necessary*)**

→ **We are not using pixel info yet, so our Z intra-module encoding is very basic for the moment.**

Two step approach

1. Find low resolution track candidates called "roads". Solve most of the pattern recognition



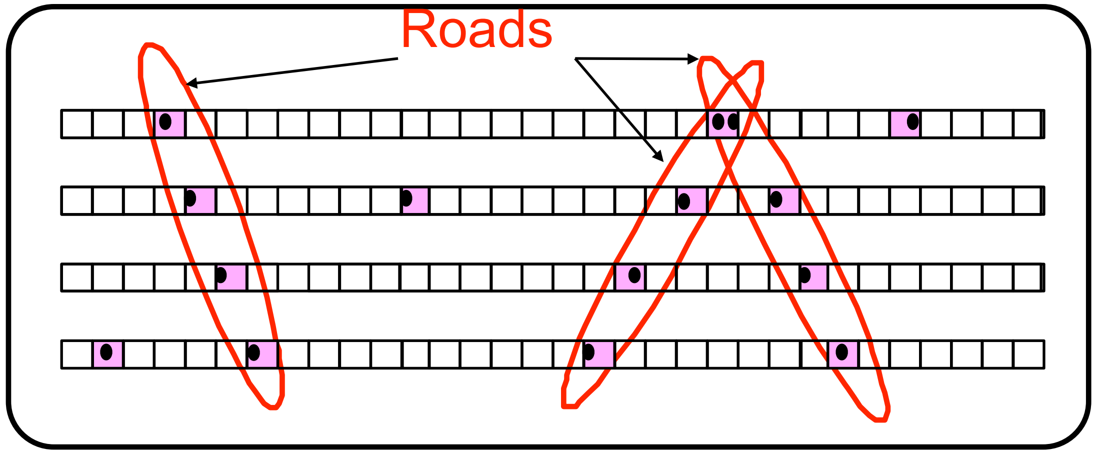
AM chip

FPGA

AM chip + FPGA

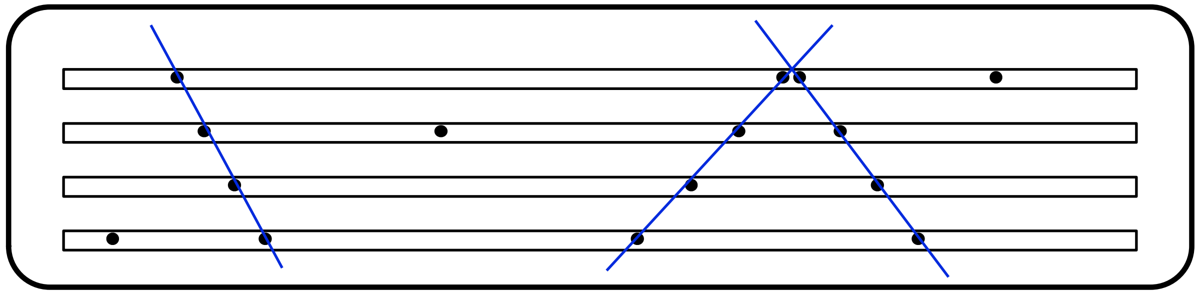
Two step approach

1. Find low resolution track candidates called “roads”. Solve most of the pattern recognition



AM chip

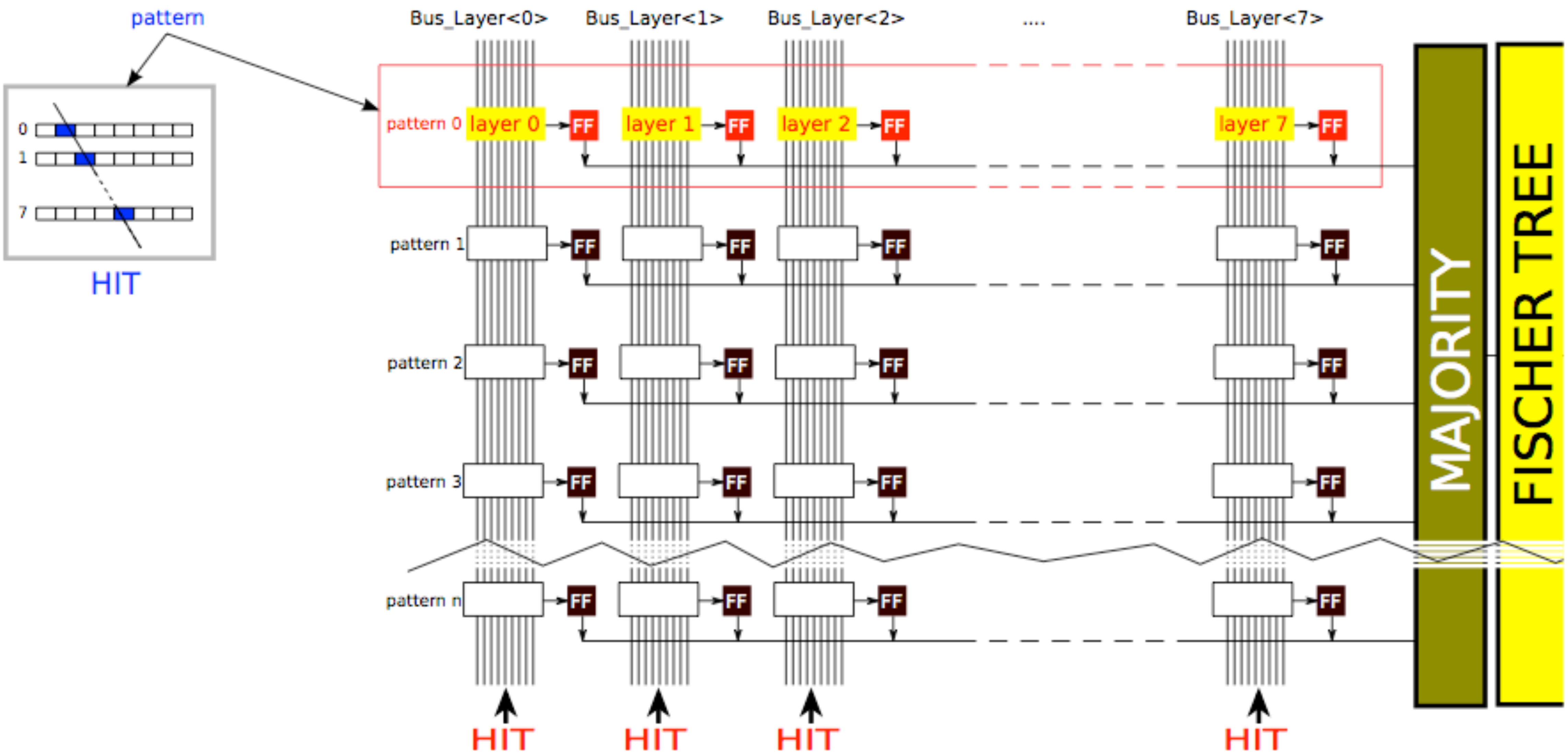
2. Then fit tracks inside roads.
   Thanks to 1st step it is much easier



FPGA

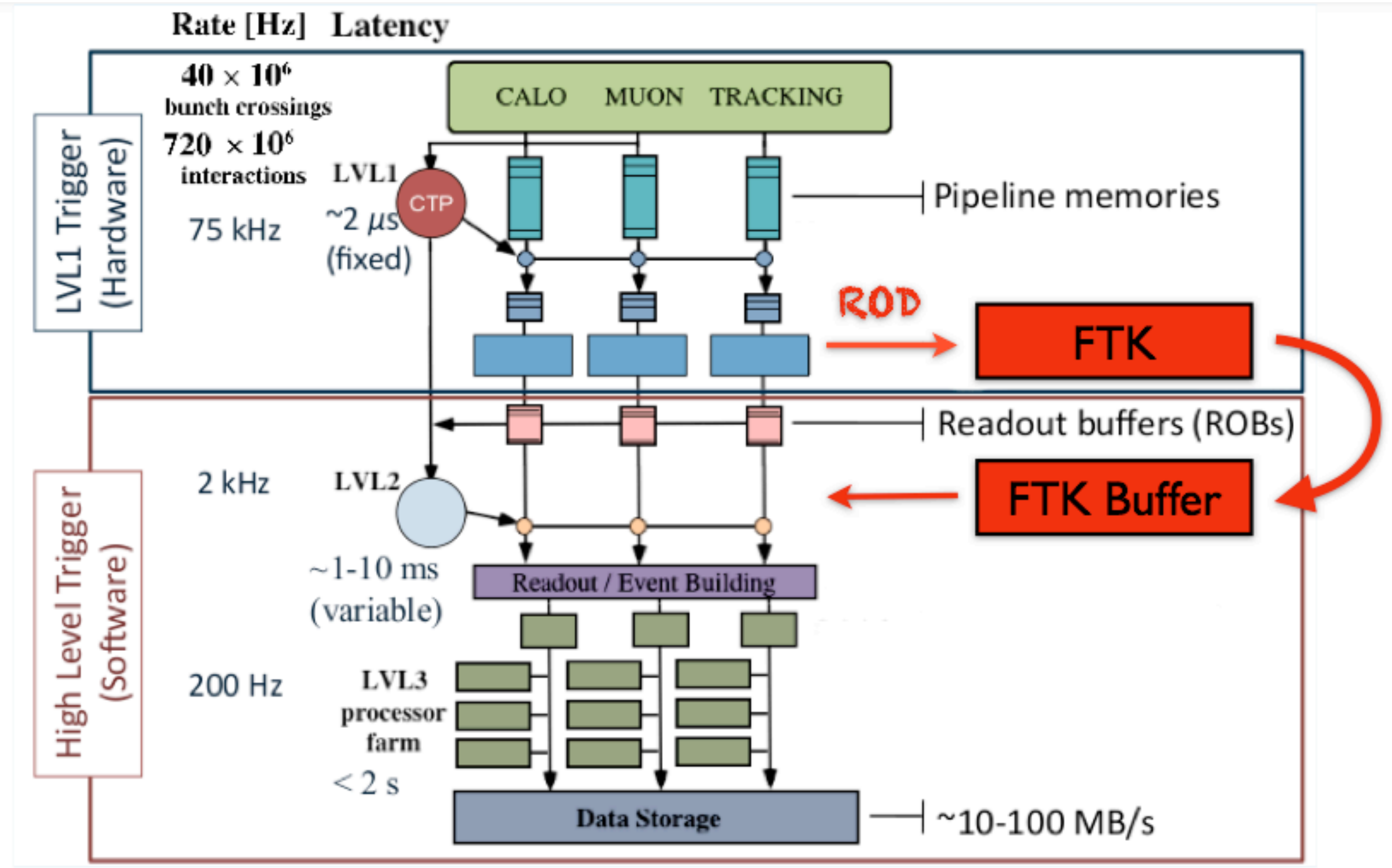
AM chip + FPGA

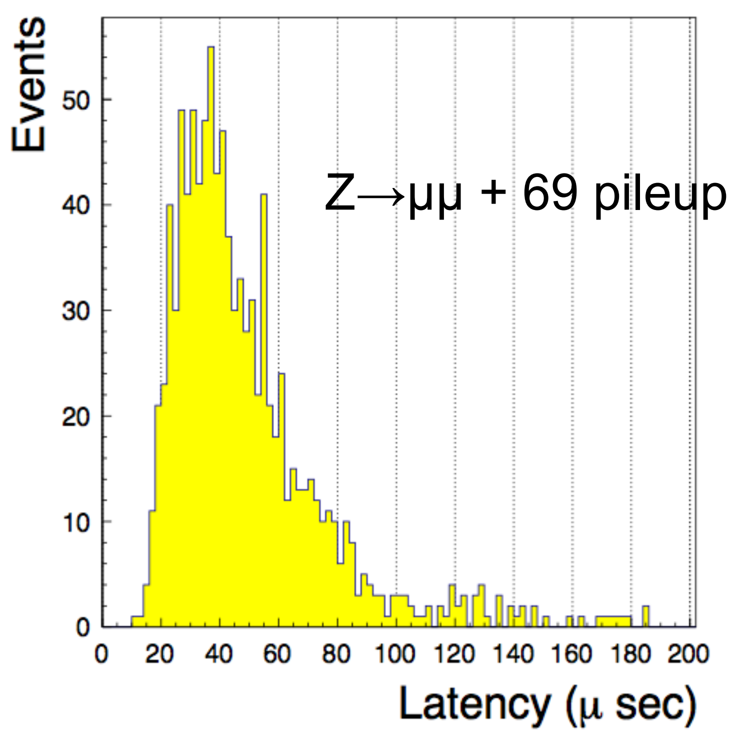
The AM chip at work



The event hit positions are received over 8 input buses of 15 bits each.
All the hits are then compared with the data stored inside each layer block, as soon as they are loaded into the chip, each one in the corresponding bus. If a layer block is matched, the corresponding Flip-Flop (FF) is set. It should be noted that each hit is fed into the memory only once. In fact the bus line transmits the information to all the layer blocks, and, if matched, all the corresponding FF are set simultaneously. **Finally, a given pattern is matched with a logic that counts the number of FF set to 1 within a row, using a majority logic: that means that one could ask a minimum number of FF set**

Usage in ATLAS @L1.5

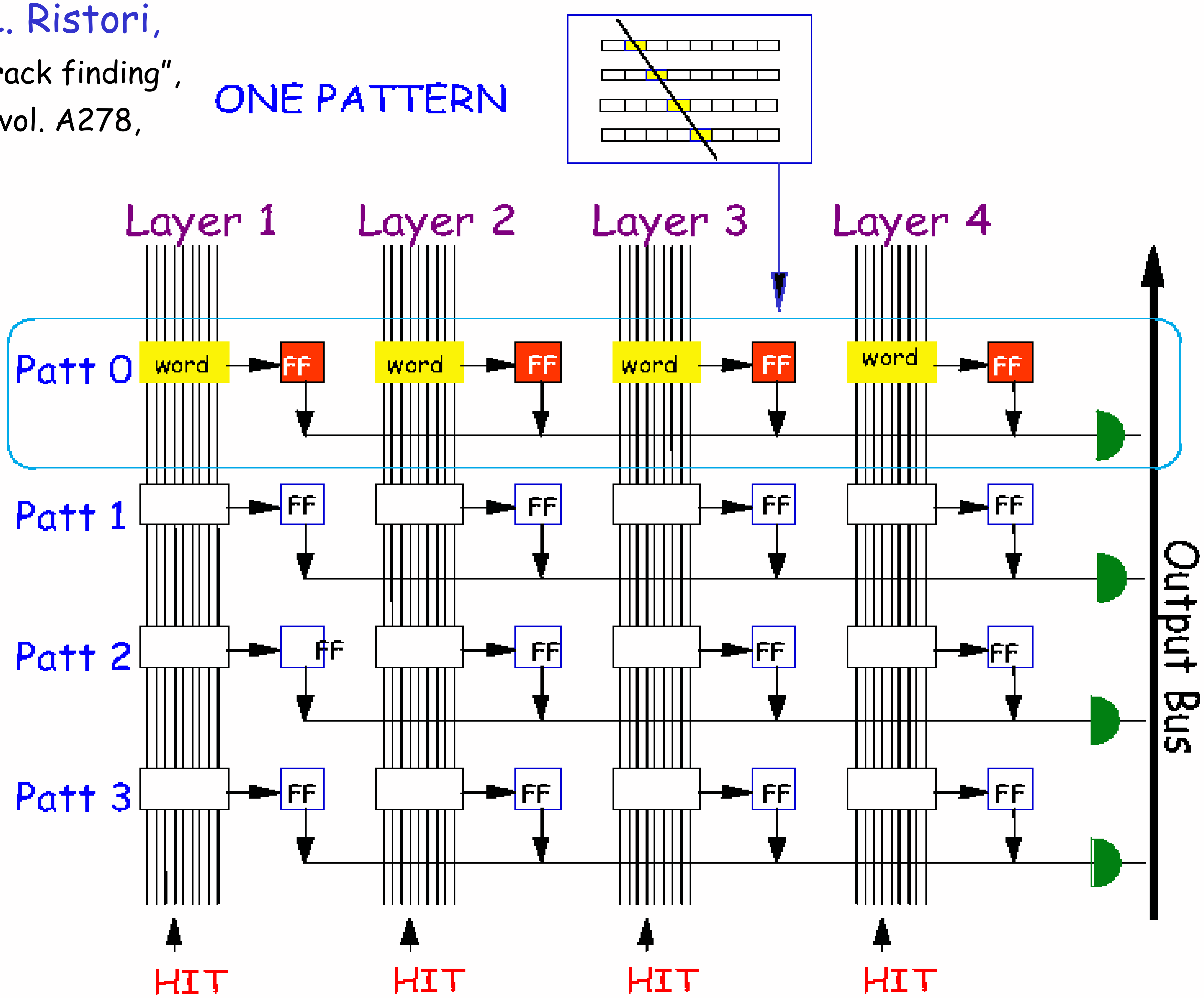




Associative Memory for pattern matching

M. Dell'Orso and L. Ristori,
"VLSI structures for track finding",
Nucl. Instr. and Meth., vol. A278,
pp. 436-440, (1989).

1 register
1 comparator
1 match FF
/ layer
/ pattern



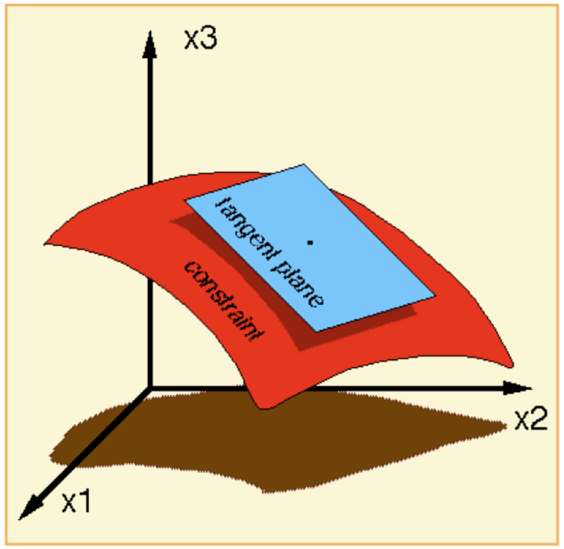
Track fitting - high quality helix parameters and χ^2

Principal component analysis

- Over a narrow region in the detector, equations linear in the local silicon hit coordinates give resolution nearly as good as a time-consuming helical fit.

Nucl.Instrum.Meth.A623:540-542,2010
doi:10.1016/j.nima.2010.03.063

$$p_i = \sum_{j=1}^{14} a_{ij} x_j + b_i$$

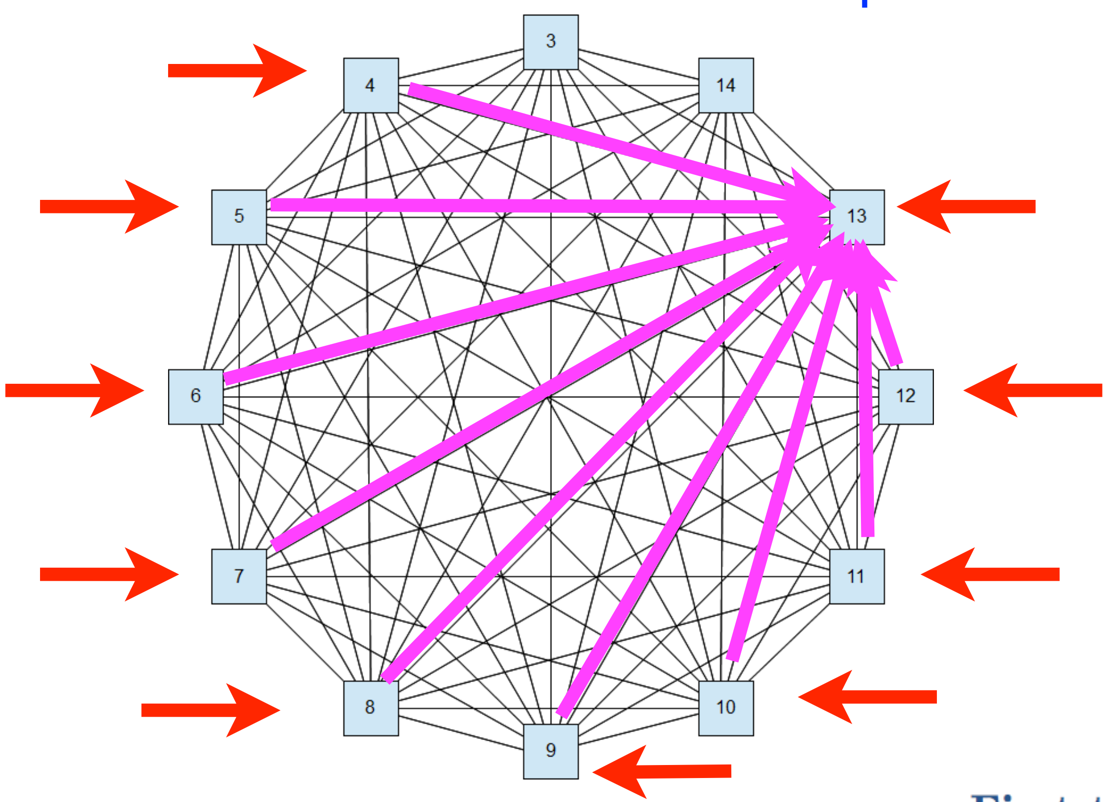


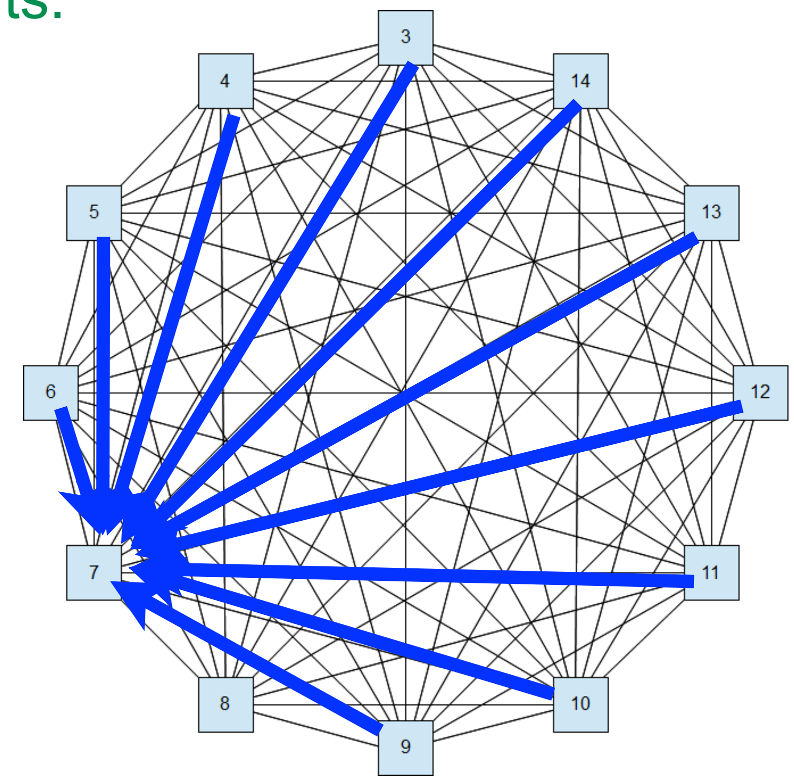
- p_i's are the helix parameters and 2 components.
- x_j's are the hit coordinates in the silicon layers.
- a_{ij} & b_i are pre-stored constants determined from full simulation or real data tracks.
- The range of the linear fit is a "sector" which consists of a single silicon module in each detector layer.
- This is VERY fast in FPGA DSPs.

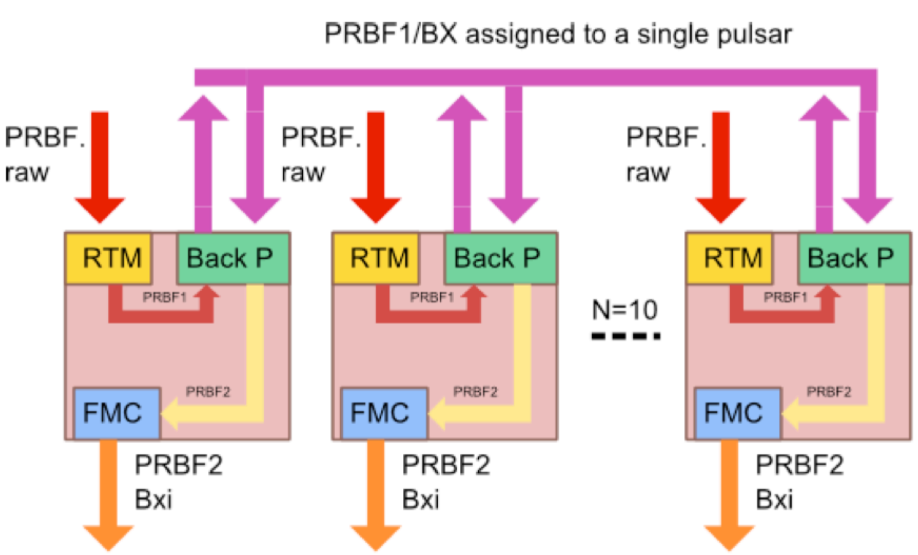
- ~few hundred fitting engines/trigger sector for CMS

Time multiplexing and data formatting

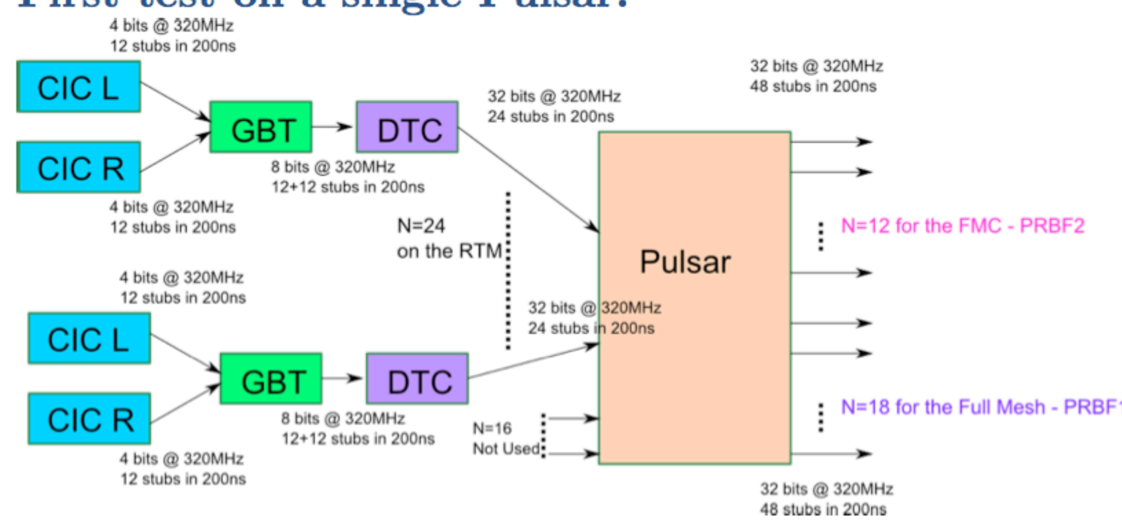
Ten processors send data to target processor blade in round robin scheme.
Each blade will have a few mezzanines to handle multiple events.
Does not need to wait last stub inputed to start track finding.







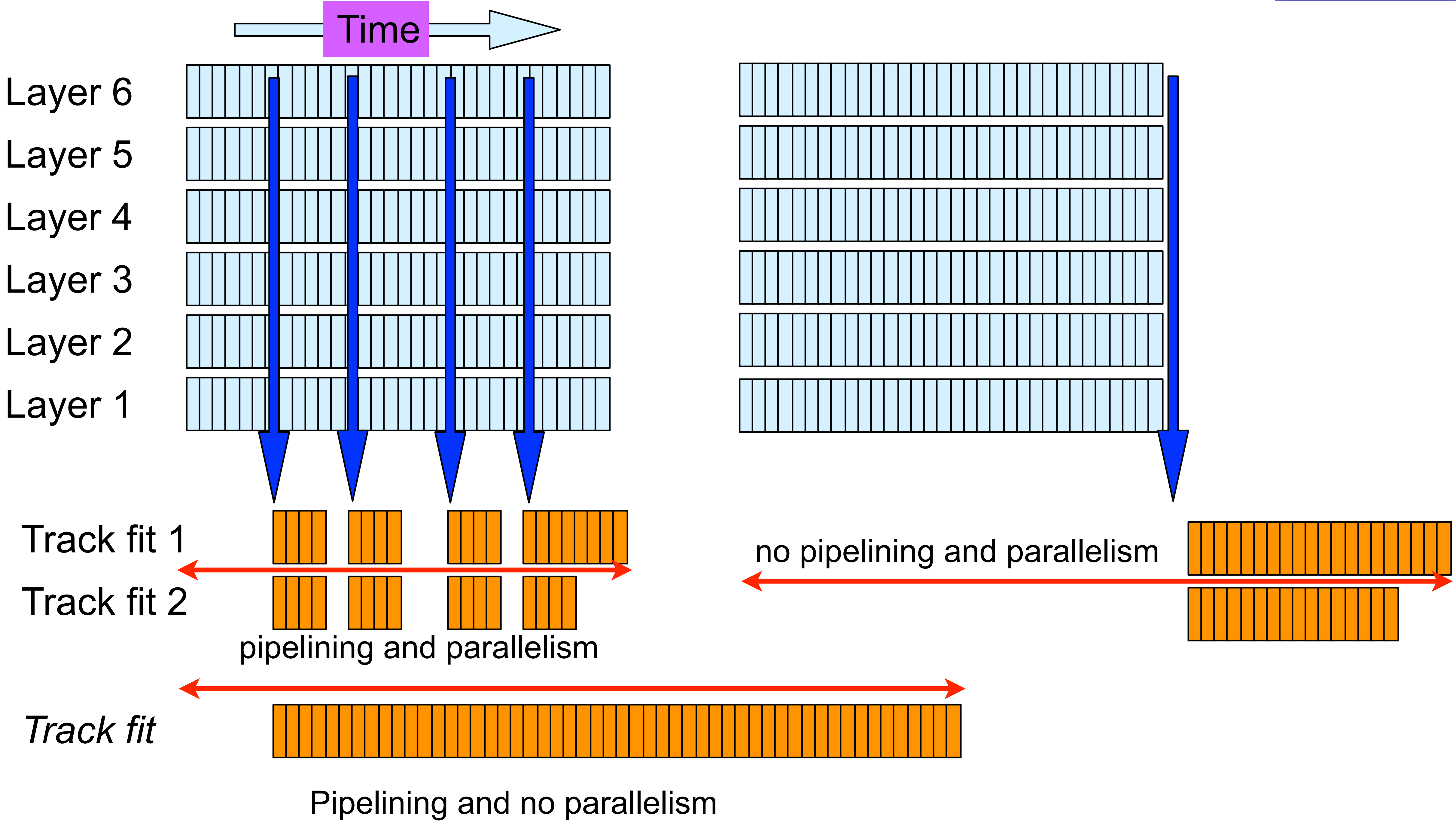
First test on a single Pulsar:



Minimal requirements on DTC

Preliminary Latency ~1 μs

Latency, pipelining and parallelism



FTK example (no pipeline and parallelism)

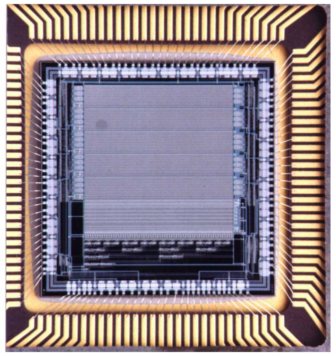
typical layer 500 hits in input @10 ns each => 5 μs

50 roads output @ 10 ns each => 0.5μs

x 4 fitters in parallel @ 2 ns /fit; hottest road with 16 fits => 160 ns

AM technological evolution

SVT
AM chip



- (90's) **Full custom VLSI chip -** 0.7μm (INFN-Pisa)
- **128 patterns, 6x12bit words each, 30MHz**

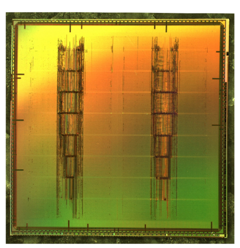
F. Morsani et al., IEEE Trans. on Nucl. Sci., vol. 39 **(1992)**

Alternative **FPGA** implementation of SVT AM chip

P. Giannetti et al., Nucl. Intsr. and Meth., vol. A413/2-3, **(1998)**

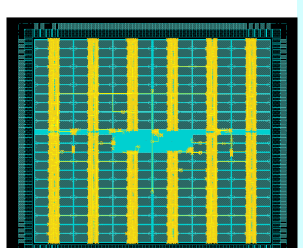
G Magazzù, 1st std cell project presented @ LHCC (1999)

SVT upgrade



Standard Cell 0.18 μm → 5000 pattern/AM chip
SVT upgrade total: 6M pattern, 40MHz
A. Annovi et al., **IEEE TNS**, Vol 53, Issue 4, Part 2, **2006**

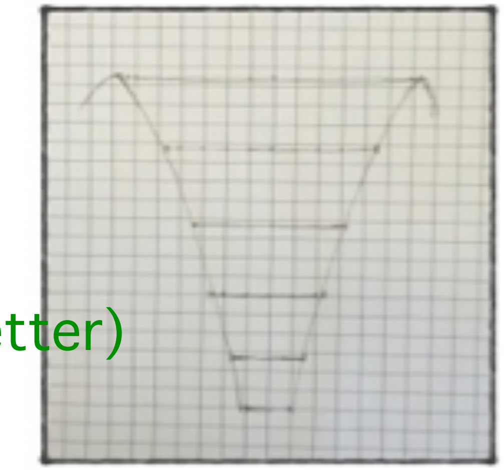
FTK R&D

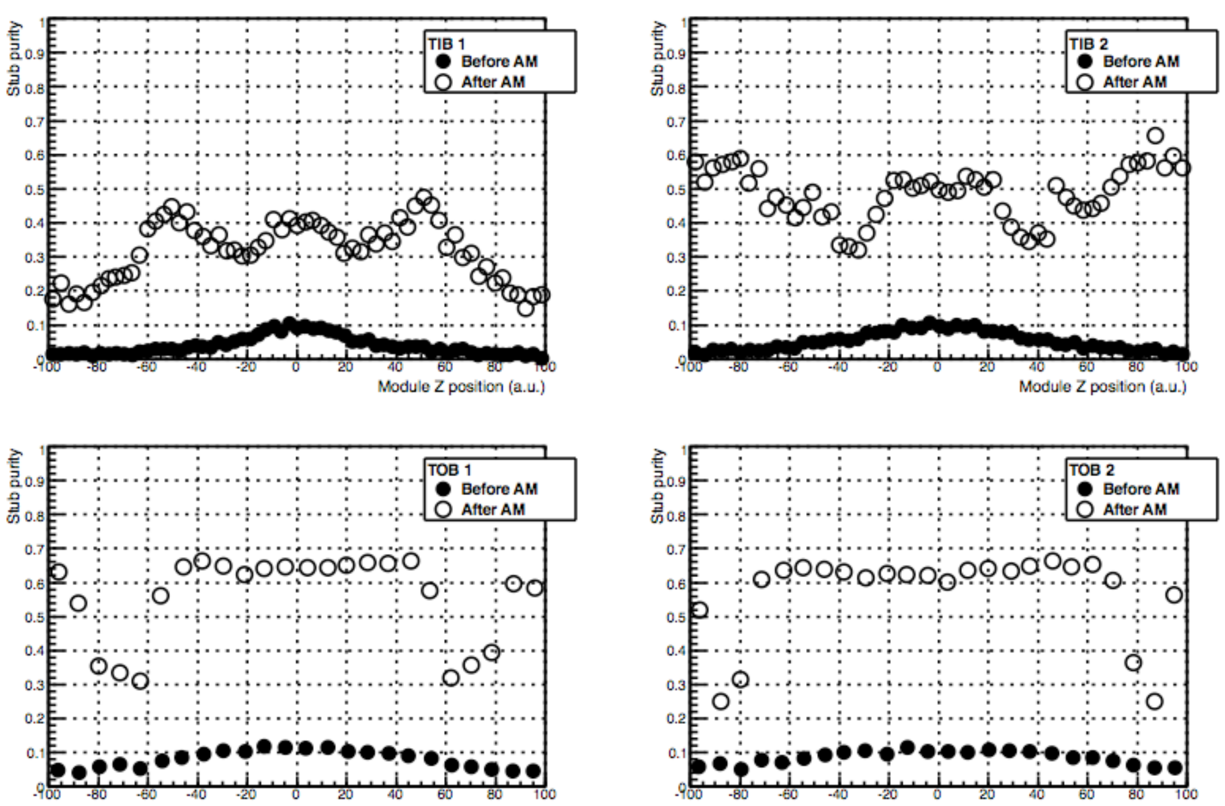


AMchip04 –65nm technology, std cell & full custom, 100MHz
Power/pattern/MHz ~30 times less. Pattern density x12.
First variable resolution implementation!
F. Alberti *et al 2013 JINST* ***8 C01040***, ***doi:***10.1088/1748-0221/8/01/C01040

System dimensioning

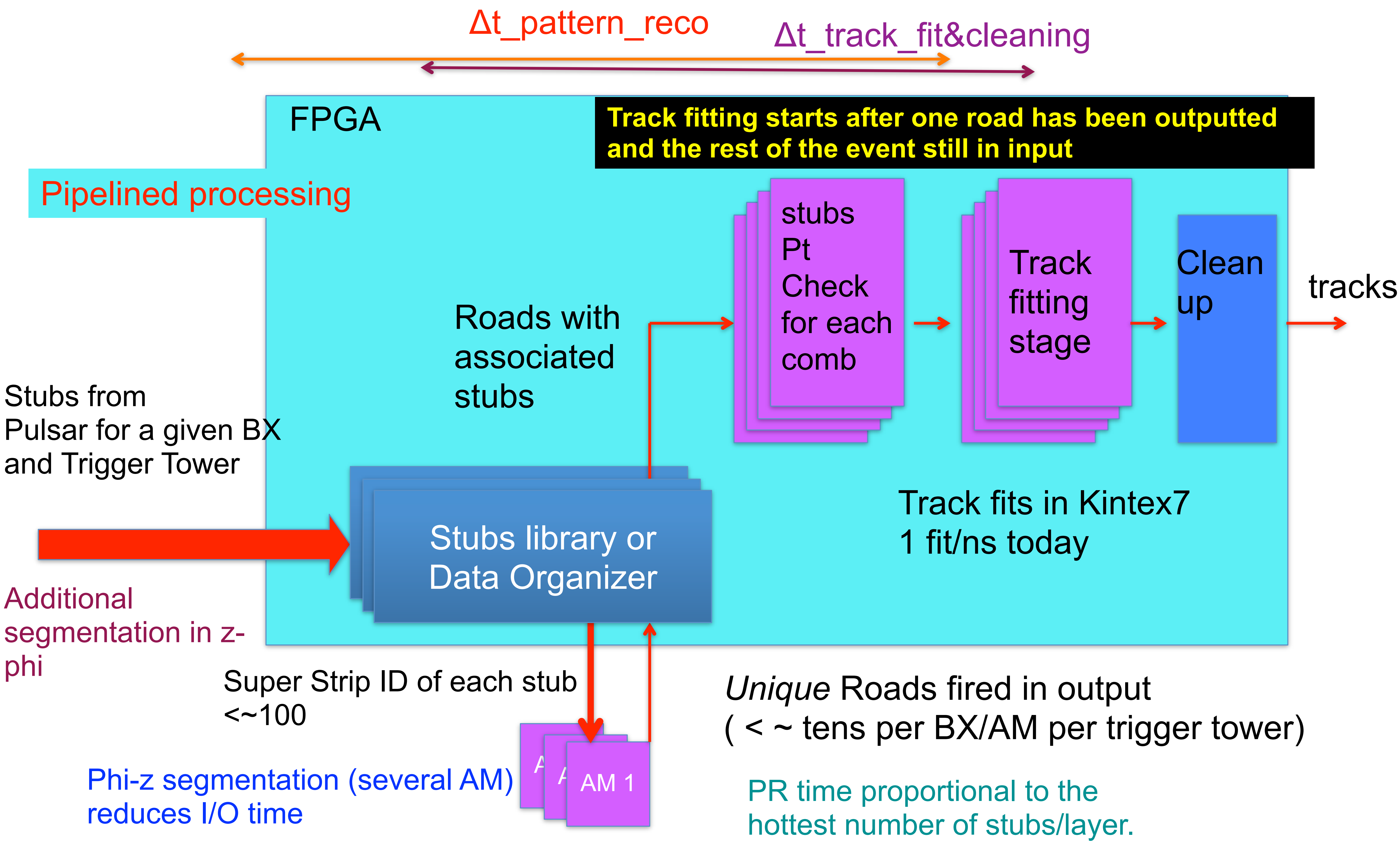
- Pattern matching
  - Optimization on-going
    - fixed super-strip (32 strips each) size for all layers: ~4 M patterns
    - projective (8/16/32 …) sizable reduction (up to 2); ~same (or even better) performance
  - Unique roads fired per trigger ~<50 @ PU 200 and 3 GeV threshold
  - Efficiency (μ, electrons)~99%
  - Purity of stubs after AM filtering ~60%
  - Further ~30% gain from stub pT info



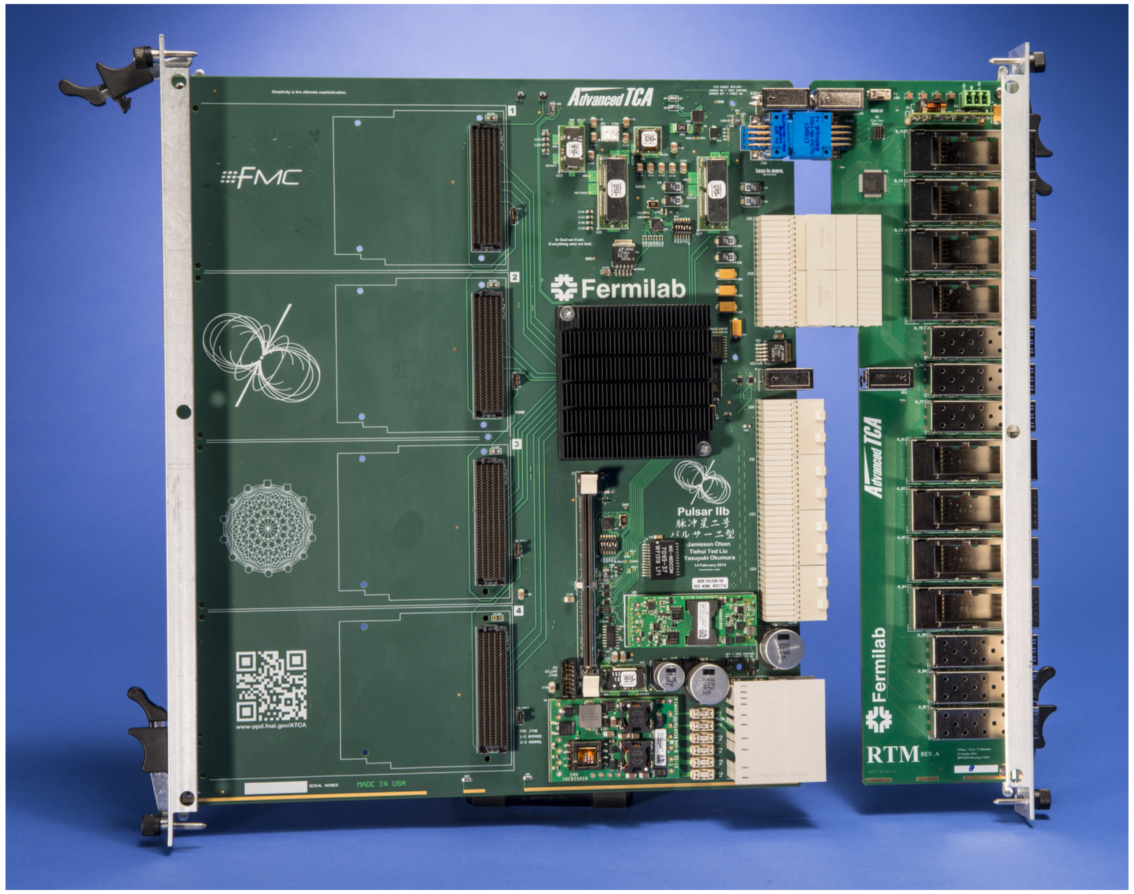


		Bank type		Δ (in %)
		Baseline	Combo	
Endcap	*Muon gun efficiency (Nhits≥5)*	98,6	98,4	-0,2
Endcap	*Electron gun efficiency (Nhits≥5)*	96,0	93,6	-2,5
Endcap	*PU140 road rate*	119,0	24,0	-79,8
Endcap	*PU140 fake road proportion*	52,8	31,7	-40,0
Endcap	*PU200 road rate*	216,0	38,0	-82,4
Endcap	*PU200 fake road proportion*	62,0	41,7	-32,7
Hybrid	*Muon gun efficiency (Nhits≥5)*	98,5	97,5	-1,0
Hybrid	*Electron gun efficiency (Nhits≥5)*	97,6	95,6	-2,0
Hybrid	*PU140 road rate*	248,0	35,0	-85,9
Hybrid	*PU140 fake road proportion*	73,7	48,4	-34,3
Hybrid	*PU200 road rate*	534,0	61,0	-88,6
Hybrid	*PU200 fake road proportion*	83,7	65,6	-21,6
Barrel	*Muon gun efficiency (Nhits≥5)*	99,0	98,6	-0,4
Barrel	*Electron gun efficiency (Nhits≥5)*	98,5	97,3	-1,2
Barrel	*PU140 road rate*	201,0	36,0	-82,1
Barrel	*PU140 fake road proportion*	62,4	24,9	-60,1
Barrel	*PU200 road rate*	416,0	51,0	-87,7
Barrel	*PU200 fake road proportion*	75,0	41,8	-44,3

Pattern Recognition Engine flow



Hardware



Pulsar 2b in hand
Fully qualified for 10Gb/s speed

Mezzanine in hand
being qualified for AM05/06

Other version in production
for ProtoVipram

AM chips status and prospects

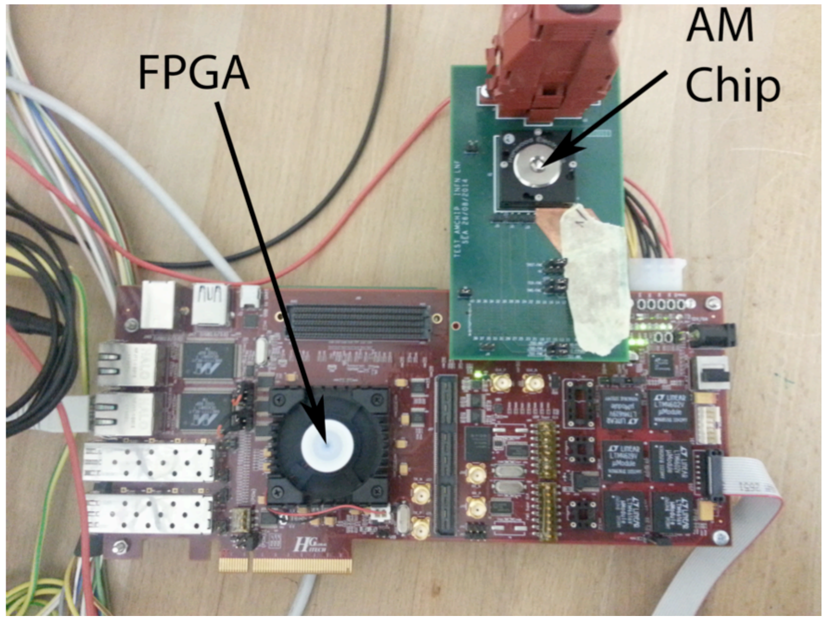
State of the art and immediate R&D

- INFN/IN2P3 65 nm AM05 (3k patterns) in hand to produce 4 mezzanines x 16 chips and AM06 (128k patterns) procurements Fall 2015.

https://indico.cern.ch/event/354340/contribution/0/material/slides/0.pdf

    - 8 input, 1 output serial lines @ 2 Gbps, 100 MHz
    - Sufficient to test latency and projections - small ratio matched roads to input stubs

- Started R&D for 28 nm, target 0.5M pattern, 200+MHz speed - not for demonstrator



- Also a dozen of FNAL protoVipram 4k pattern, 130 nm
- Started R&D on a 40 nm chip, 0.5M patterns, 200+MHz speed - not for demonstrator

AM05, its Test Stand, and AM06

Design: Stabile (MI) – Crescioli (LPNHE) – Beretta (LNF)

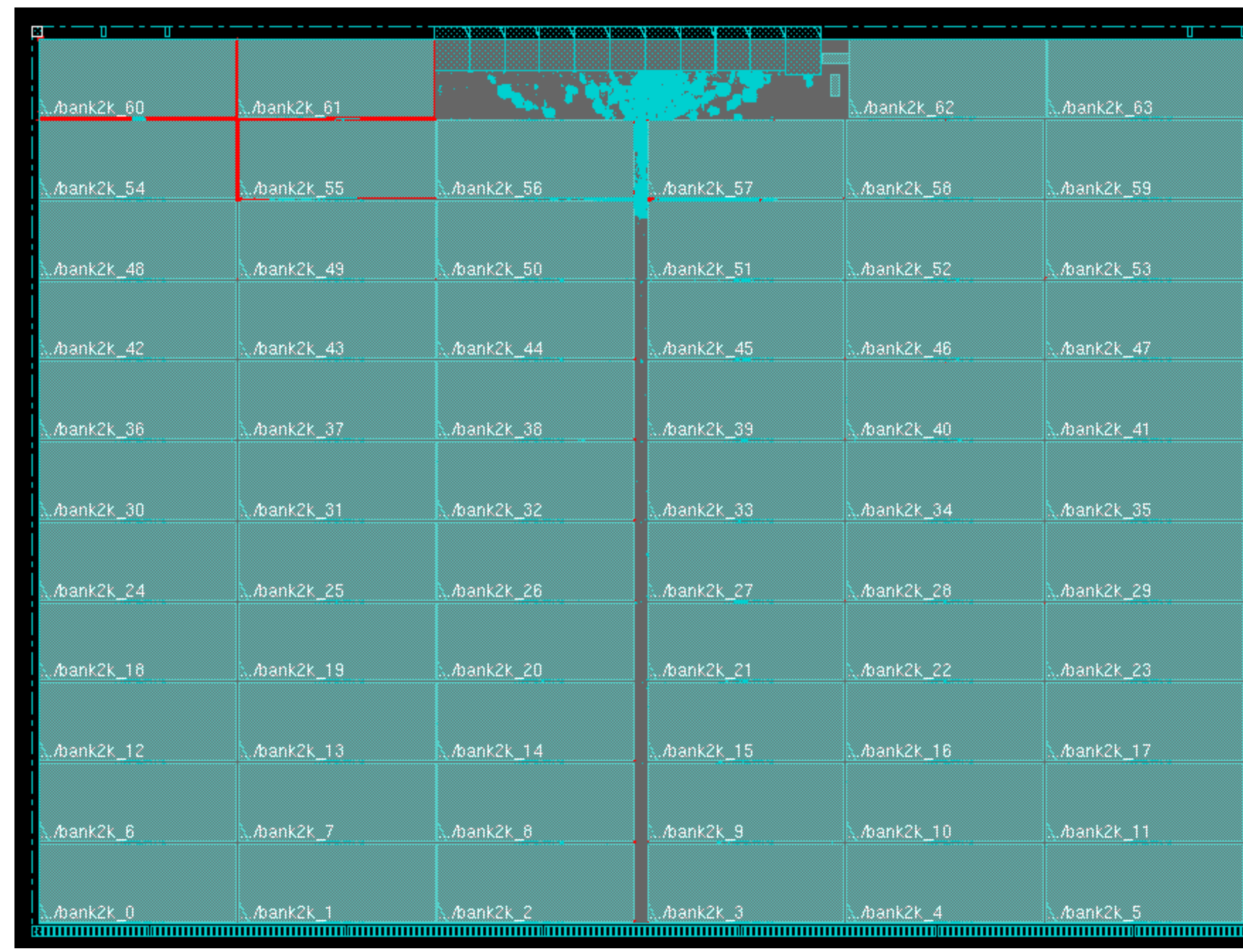
Big improvements in AMchip design

- AMchip04 power consumption / # of bit / MHz decreases of a **factor ~28** w.r.t. AMchip03
- AMchip04 memory density (patterns*layers/area) increase of a **factor ~18** w.r.t. AMchip03
- High speed serial links (11 times 2 Gb/s)

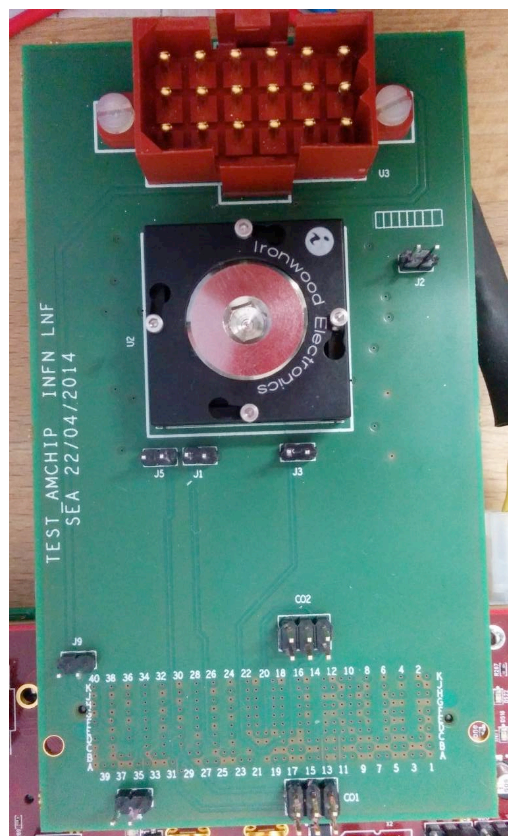
AM06 New **layout 128 kpatt**

(Stabile work, Stabile/Liberali cell)

14.6 mm x 10.8 mm^2



23x23 mm2 BGA for AM05: 3k patterns and AM06: 128k patt.



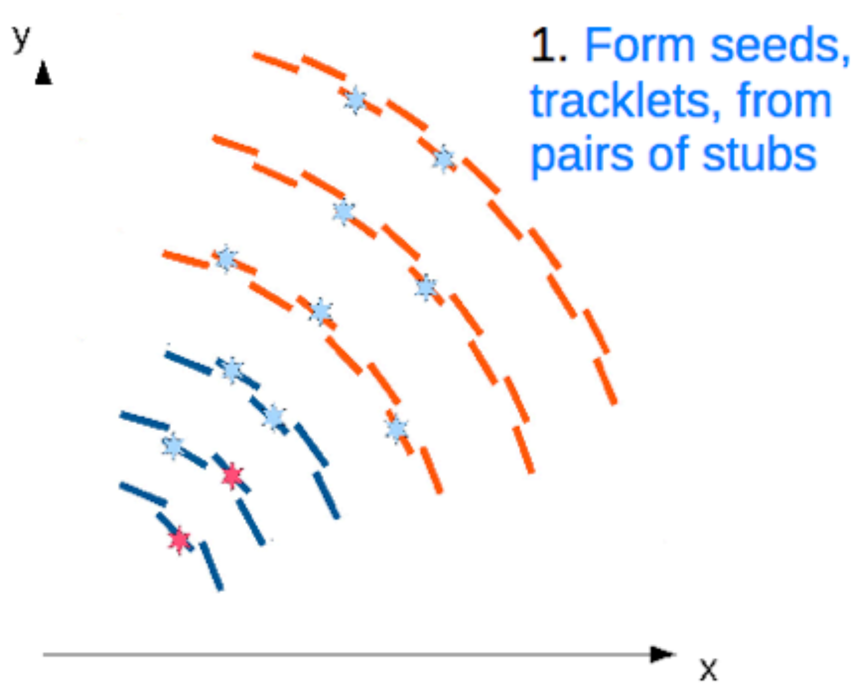
See for full information:
https://agenda.infn.it/getFile.py/access?contribId=10&sessionId=1&resId=0&materialId=slides&confId=8420

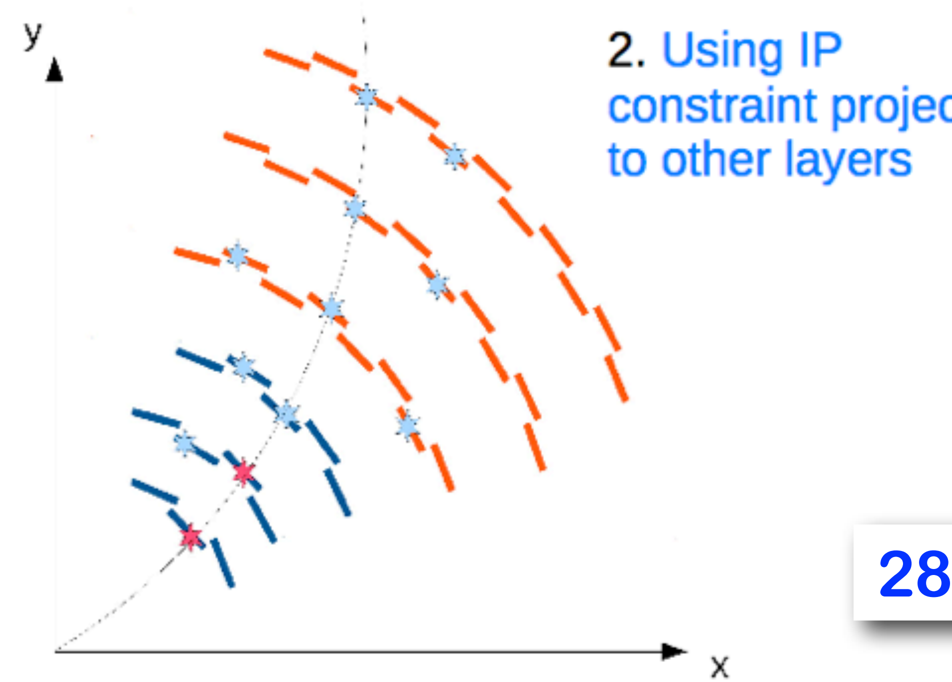
The AM chip up to 2020 – R&D

AM Chip	Year	Density (No. Mbits)	Working Frequency (MHz)	Power (W)	Voltage (V)	Technology	Area (cm^2)
AM03	**2004**	**0.5**	**40**	**1.26**	**1.8**	**180 nm**	**1**
AM04	**2012**	**1.18**	**100**	**3.70**	**1.2**	**65 nm**	**0.12**
AM06	**2014**	**18.9**	**100**	**2-3**	**1.0/0.8**	**65 nm**	**1.6**
AM2020	**2020?**	**76?**	**200+**	**~3 @100 MHz**	**0.8**	**28 nm**	**?**

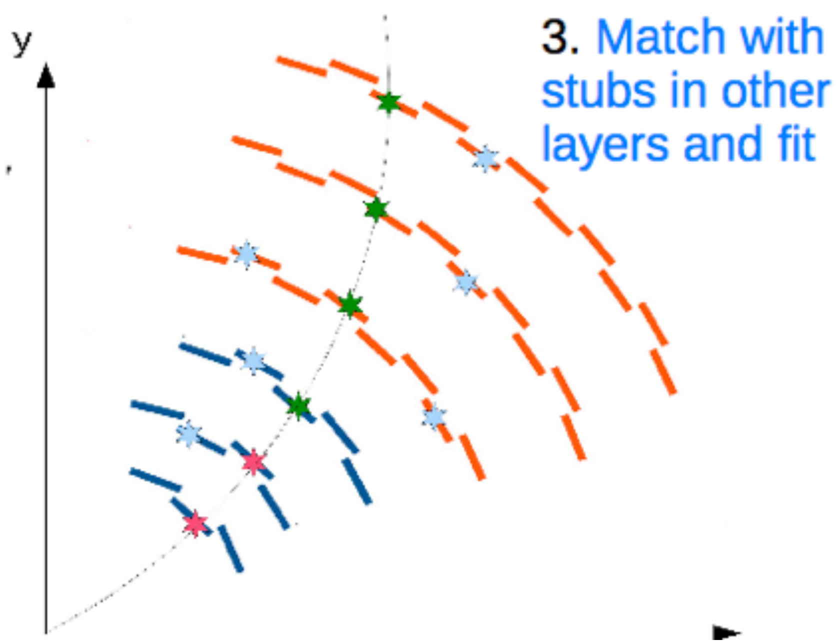
- The AM2020 chip features
  - Assuming technology scaling would allow $(65/28)^2$ ~5.4 more density
    - Conservatively target a factor 4x patterns ⇒ 0.5 M patterns
  - Need to optimize the design to decrease power consumption and area of memory arrays
    - Target ~3 W total power @100 MHz
  - Optimize latency reduction: inputs from simulations and demonstrator
    - Is 200 MHz is required to speed up I/O ? – could double the power
    - Need more output buses ?
  - In collaboration with LPNHE Paris (FTK) and Lyon under ANR project
  - Starting the design as soon as AM06 chip is submitted

Tracklet Algorithm: Road Search





28 regions in ϕ



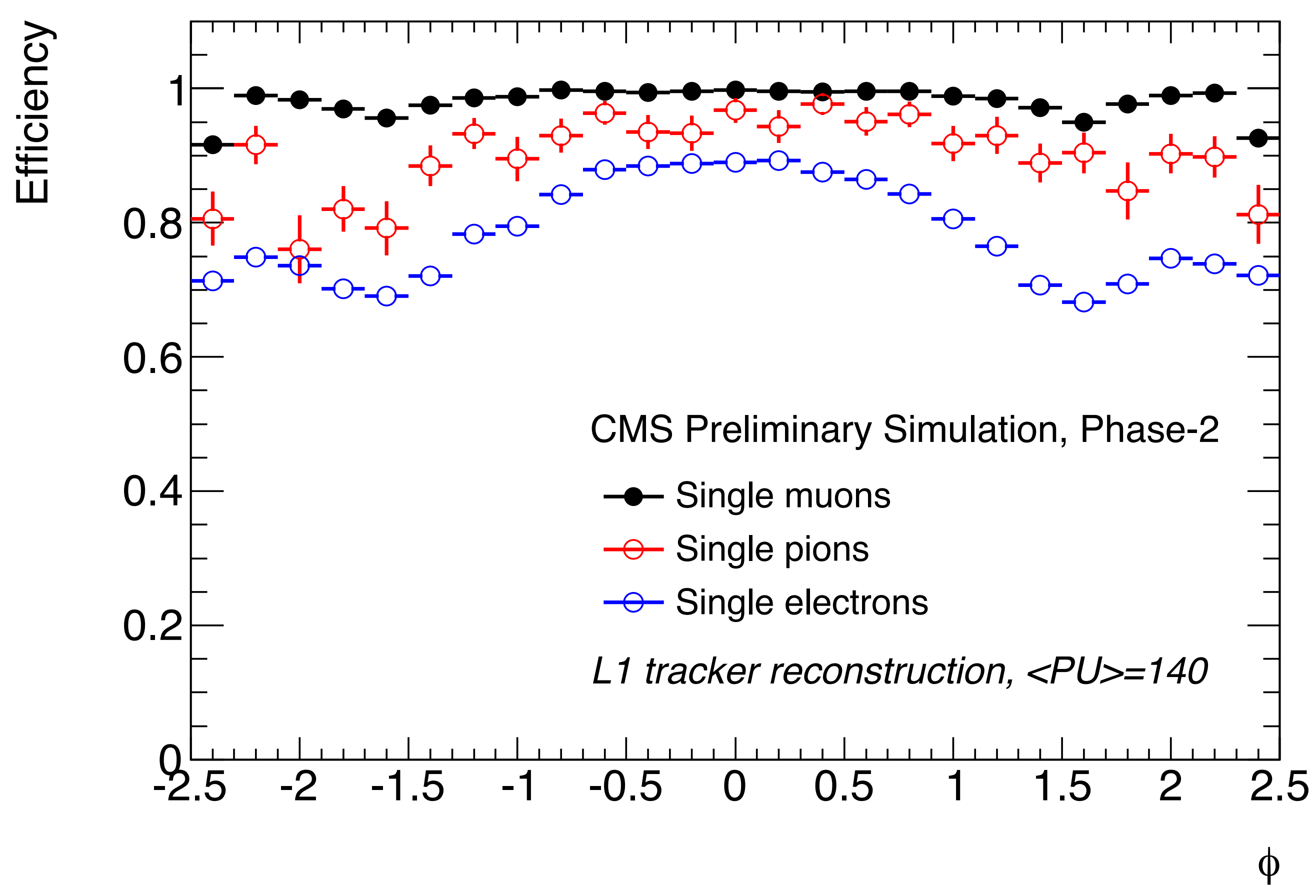
Extensive simulation program:

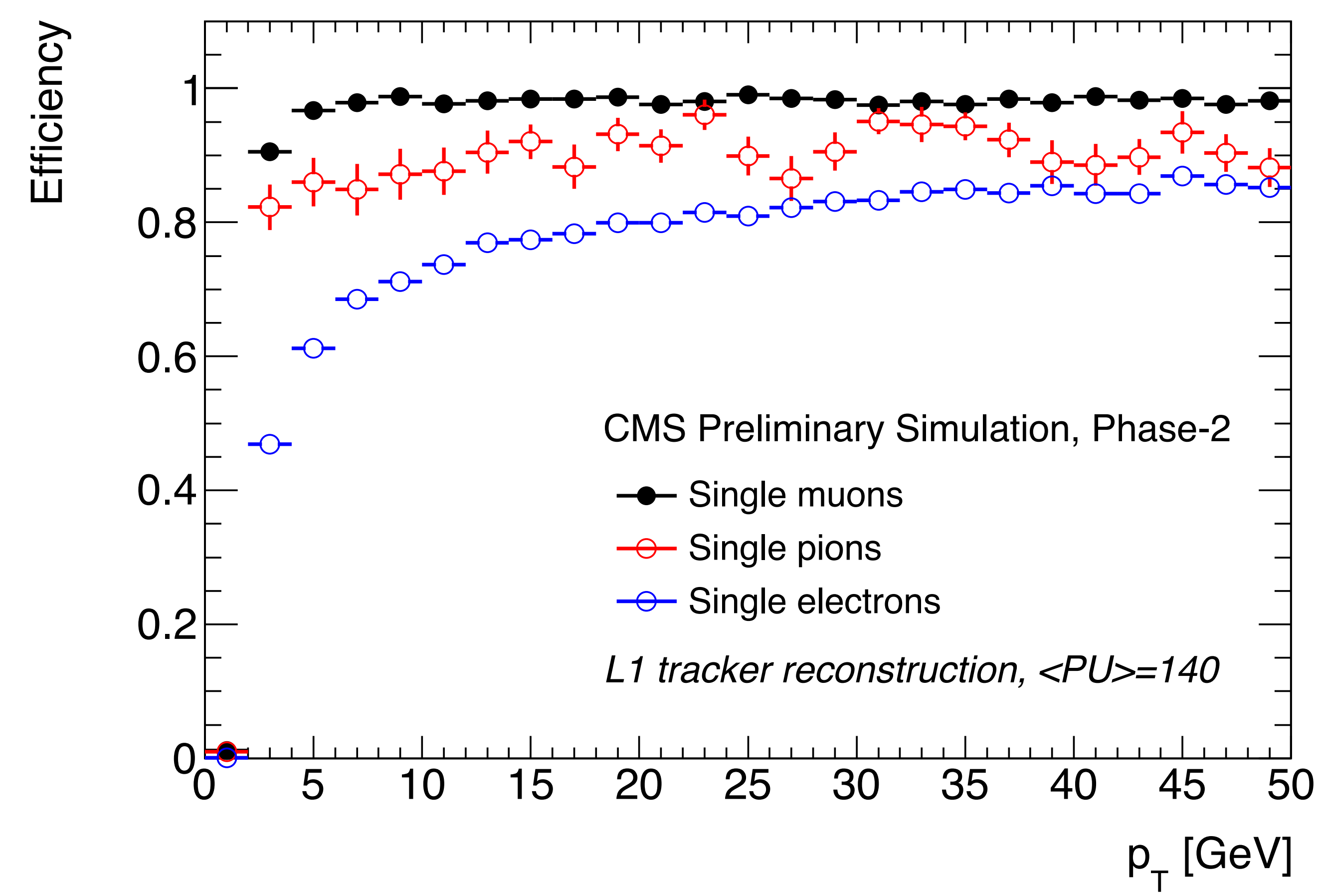
- High level simulation – used in Technical Proposal studies
- Low-level (bitwise) C++ emulation of algorithm
- Implementation in Verilog for FPGA

Shows Tracklet based algorithm performs well in HL-LHC environment

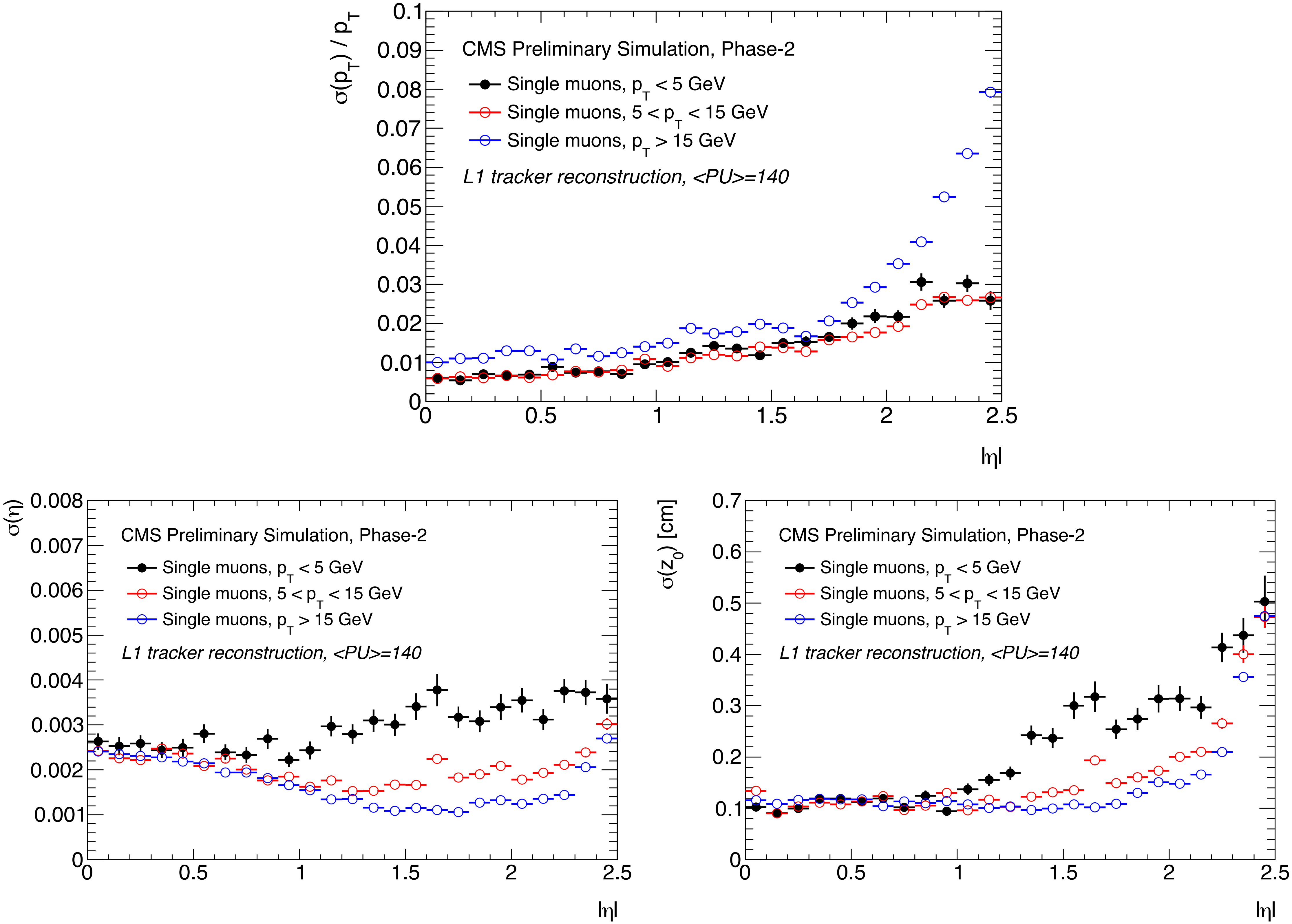
Expected performances (tracklet)

- L1 tracking efficiency as function of η & p_T for single μ, π, e with <PU>=140
  - **Muons** Sharp turn-on at 2 GeV & high efficiency across all η
  - **Pions** Somewhat lower efficiency due to higher interaction rate
  - **Electrons** Slower turn-on curve, efficiency reduced from bremsstrahlung
- For |η| < 1.0 & p_T > 2 GeV, efficiency for **μ**, **π**, **e** is **>99%**, **95%**, **87%**

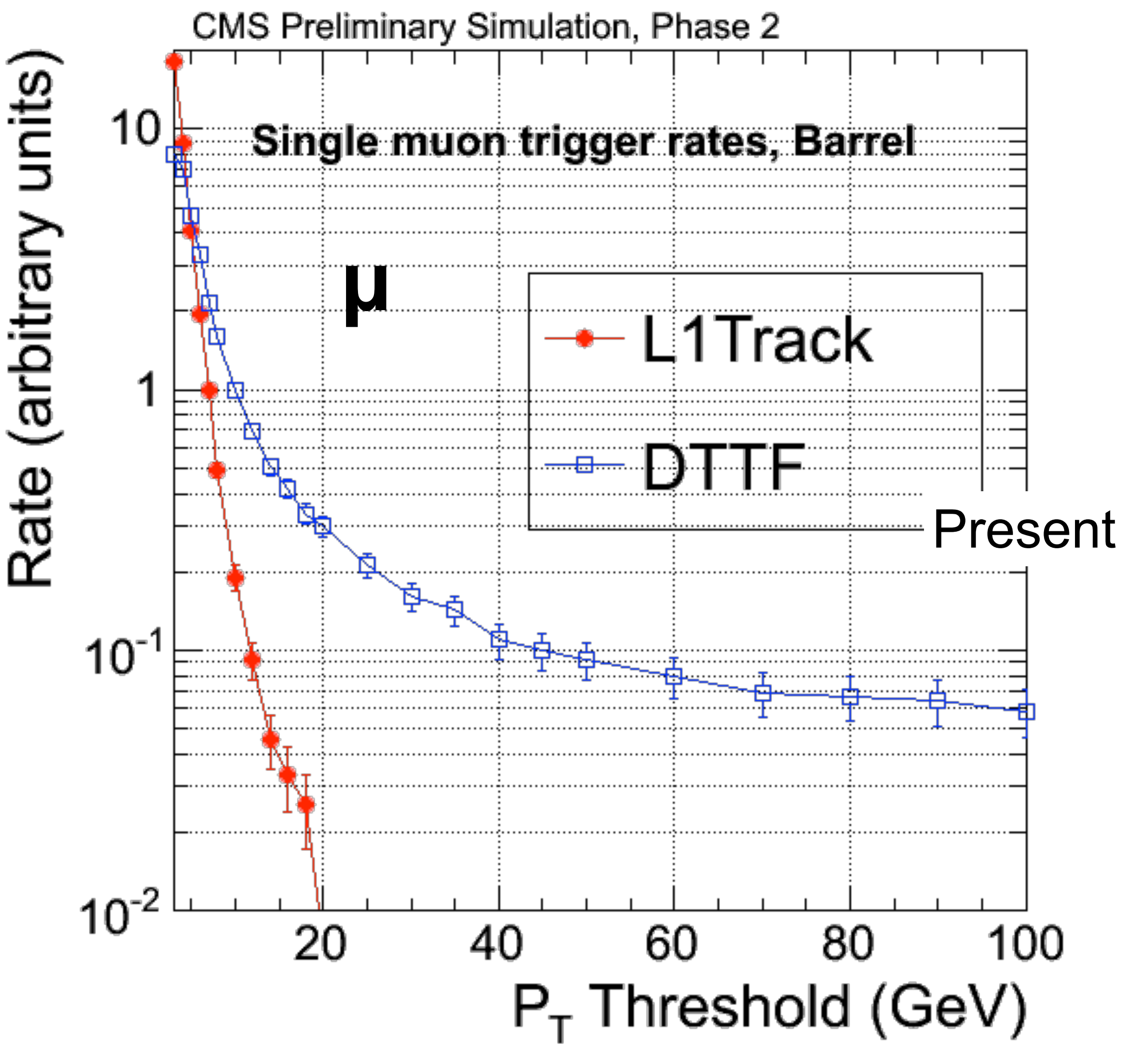


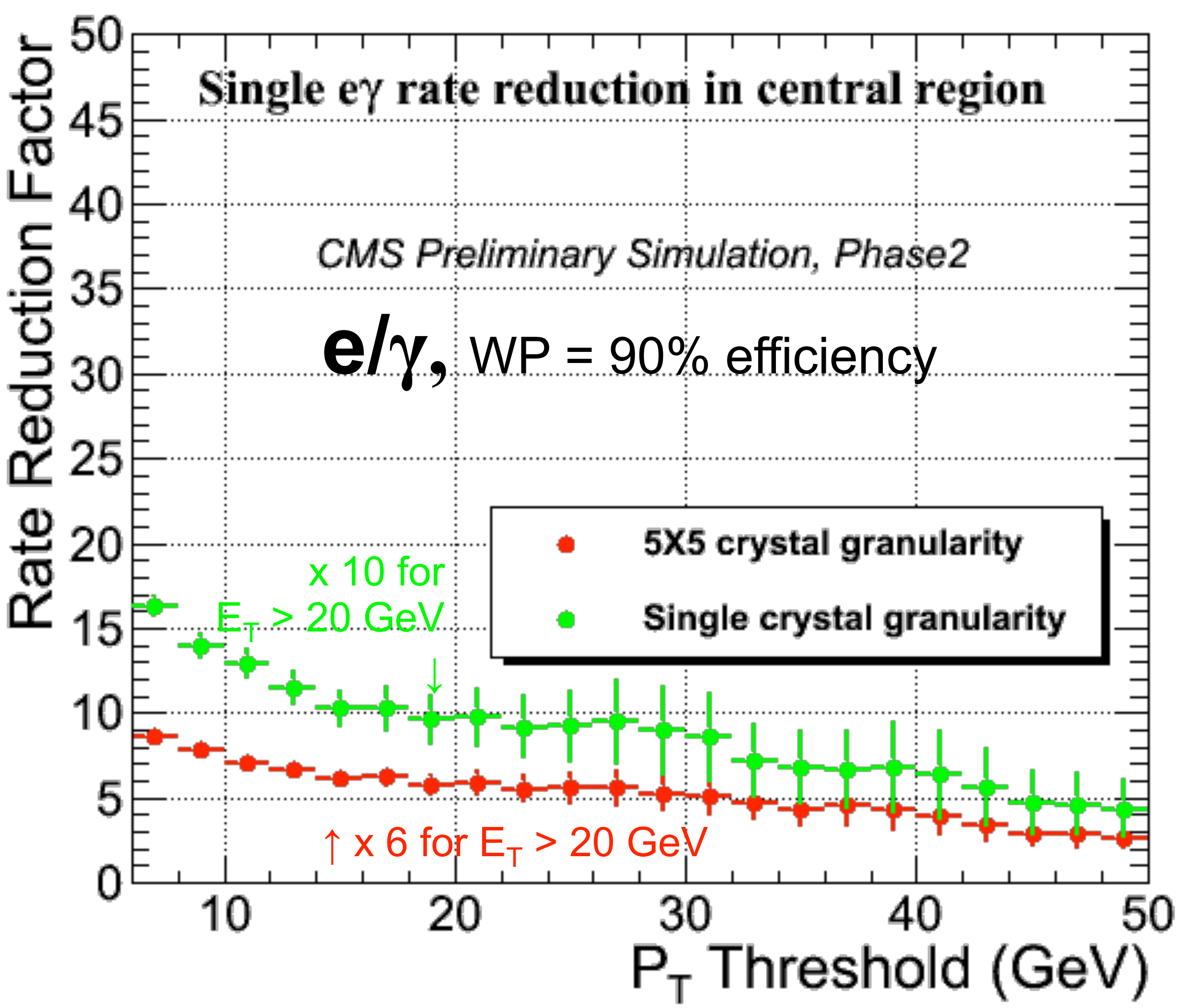


Preliminary resolutions



Usage of L1 Tracks - CMS



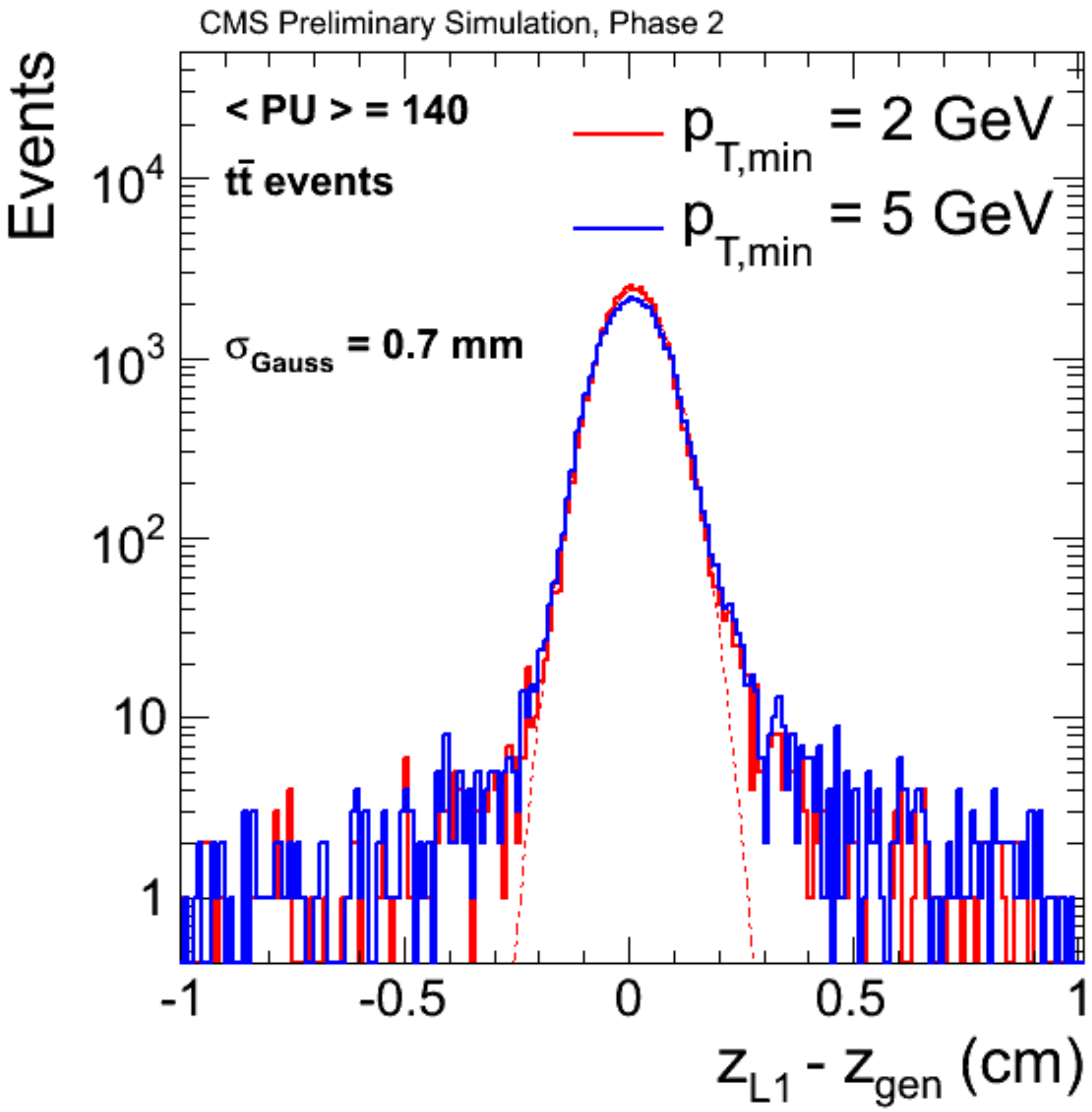


Matching Drift Tube trigger primitives with L1Tracks: **large rate reduction:**
> 10 at threshold > ~ 14 GeV. Normalized to present trigger at 10 GeV. Removes flattening at high P_t

Rate reduction brought by matching L1 e/γ to L1Track stubs for | η | < 1.
Red: with current (5x5 xtal) L1Cal granularity.
Green : using single crystal-level position resolution improves matching

Primary Vertex and Track MET

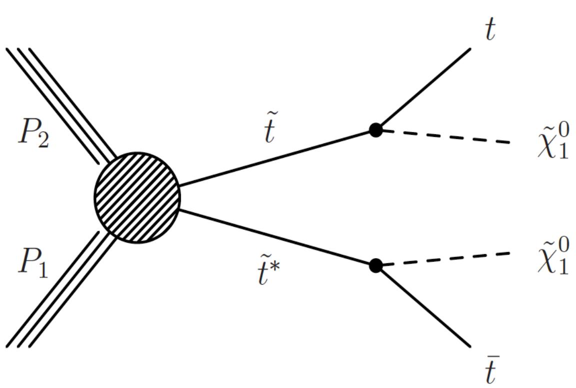
- L1 tracks can also be used to reconstruct primary vertex of event
- Resolution of primary vertex using L1 tracks with p_T > **2 GeV** or **5 GeV**
  - <1mm for events with large track multiplicity
    - *Here: ttbar <PU>=140*
  - Similar performance with the higher track p_T threshold



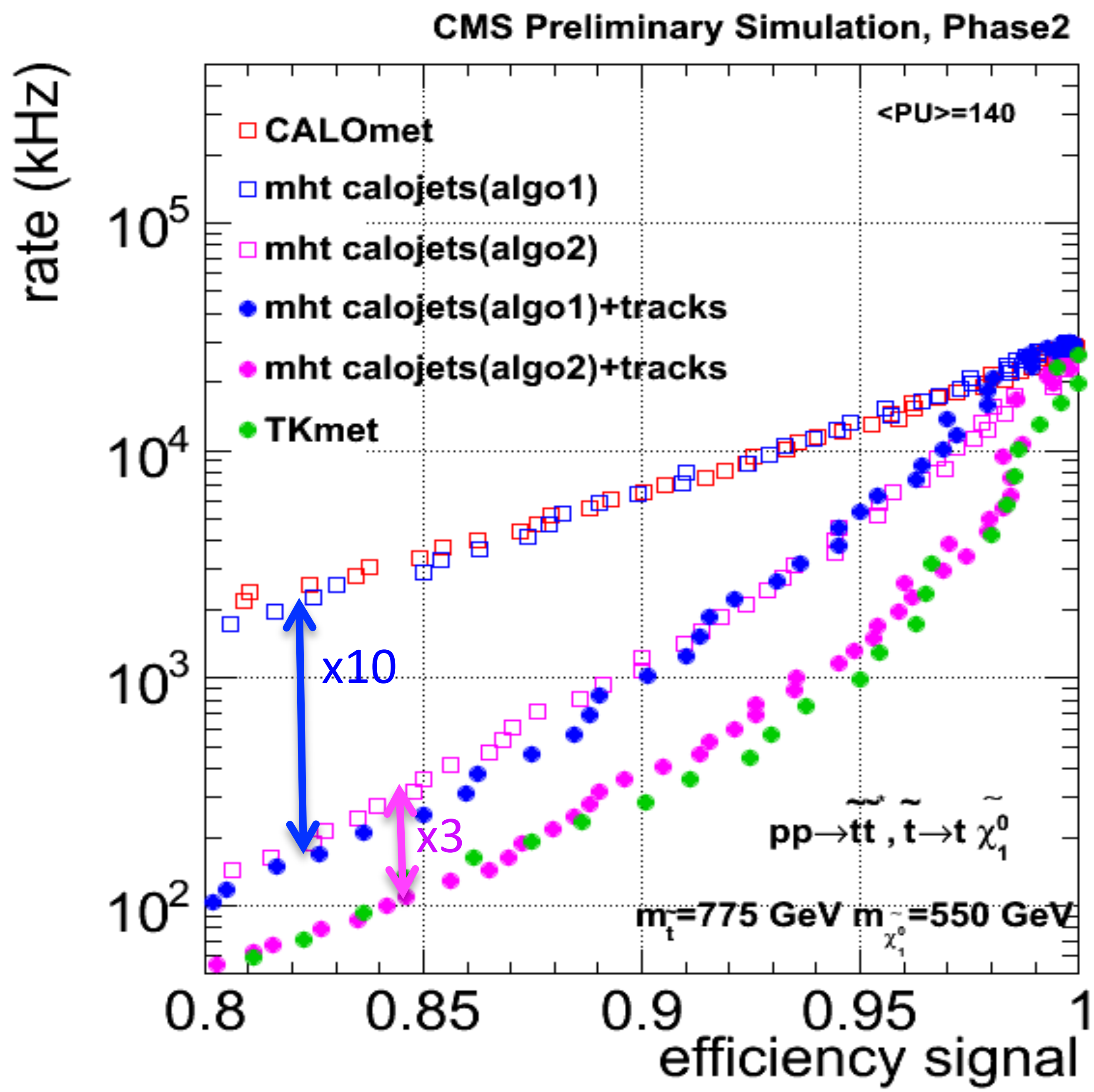
- **Track "MET"**
  - Define L1 track-based missing transverse momentum from L1 tracks coming from primary vertex

SUSY Signal point

- Rate reductions using L1 tracks for SUSY signal
  - Stop pair production with hadronic top decays (stop=775 GeV, LSP=550 GeV)
  - Signal defined by genMET > 100 GeV



- Missing H_T determined with/without vertex association
  - Algo1 & Algo2: Calorimeter-based L1 jet algorithms with different PU subtraction methods
- Sizable rate reductions achieved with tracking information!



CMS Gains from Track Trigger

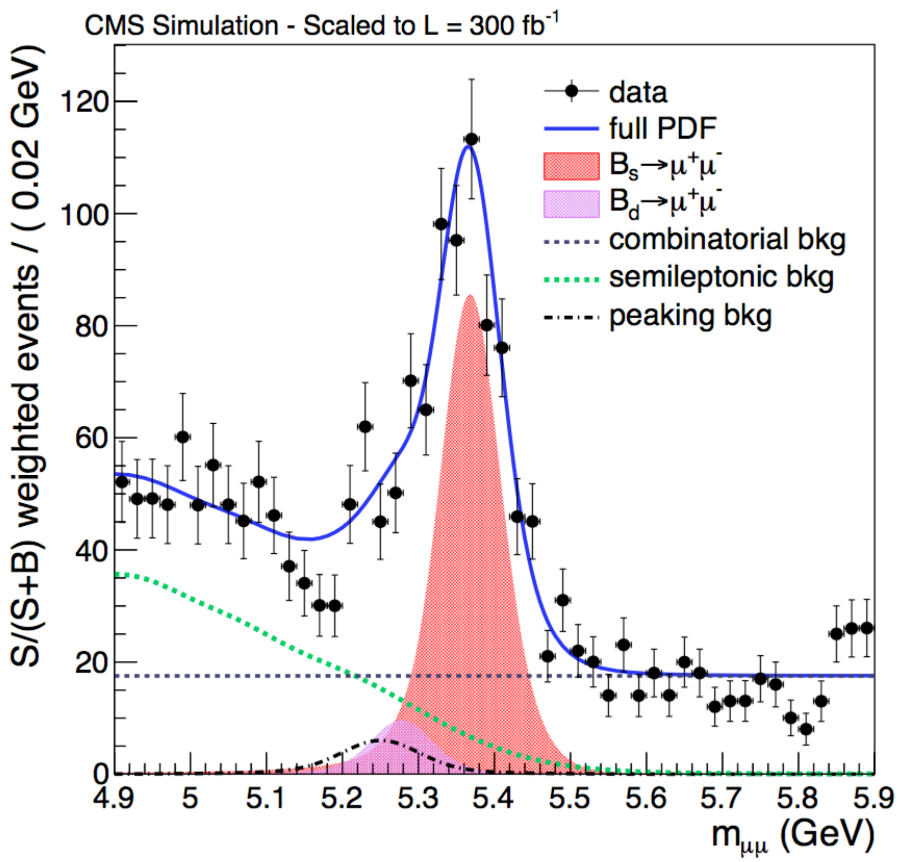
- Preliminary simulation studies demonstrate addition of L1 tracking trigger provides significant gains in rate reduction with good efficiency for physics objects. Note these results are “work in progress”.

Trigger, Threshold	Algorithm	Rate reduction	Full eff. at the plateau	Comments
Single Muon, 20 GeV	Improved Pt, via track matching	~ 13 ($\lvert\eta\rvert < 1$)	~ 90 %	Tracker isolation may help further.
Single Electron, 20 GeV	Match with cluster	> 6 (current granularity) >10 (crystal granularity) ($\lvert \eta \rvert < 1$)	90 %	Tracker isolation can bring an additional factor of up to 2.
Single Tau, 40 GeV	CaloTau – track matching + tracker isolation	O(5)	O(50 %) (for 3-prong decays)	
Single Photon, 20 GeV	Tracker isolation	40 %	90 %	Probably hard to do much better.
Multi-jets, HT	Require that jets come from the same vertex			Performances depend a lot on the trigger & threshold.

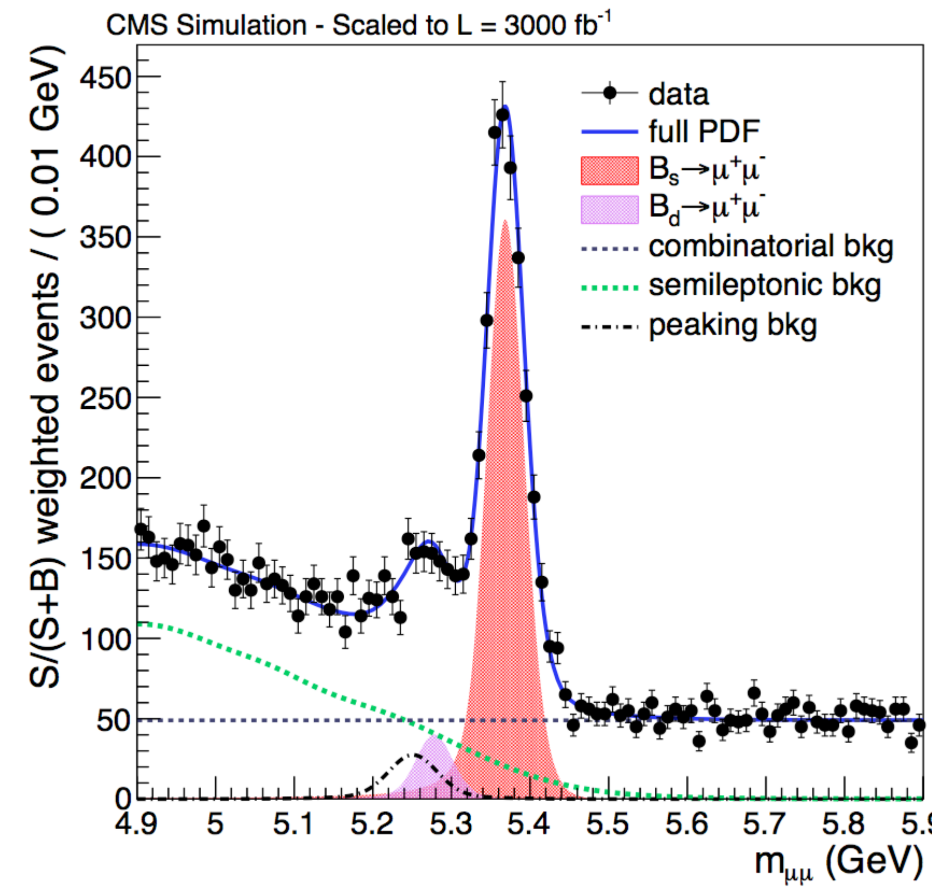
Conclusions

- Tracker information helps reducing drastically the rate of uninterested events
  - This will become a new "must" for all future detectors
- HL-LHC detectors will make use of tracking information in the Level-1 Triggers
  - Several trigger architectures exploited
    - Full readout @40 MHz, on-detector data reduction using p_T-modules
    - Implications on Tracker detector layouts ongoing
  - Some demonstrators being built to validate the full chain
  - Large gains in combining tracking with other subdetectors
    - Electrons, Muons, Jets and MET
  - High statistics of useful events for precision physics available
  - Stay tuned!

Effects on $B_{s/d} \to \mu\mu$



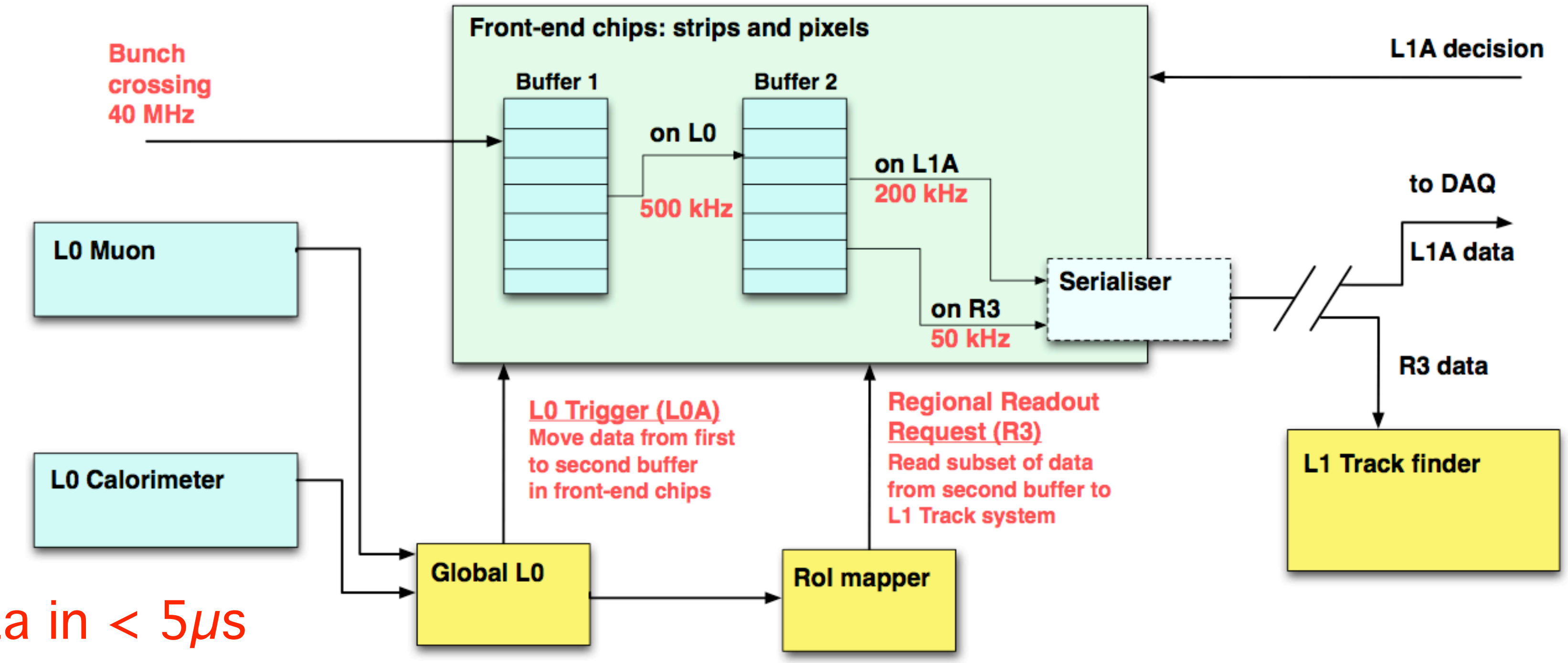
CMS PAS
FTR-13-022



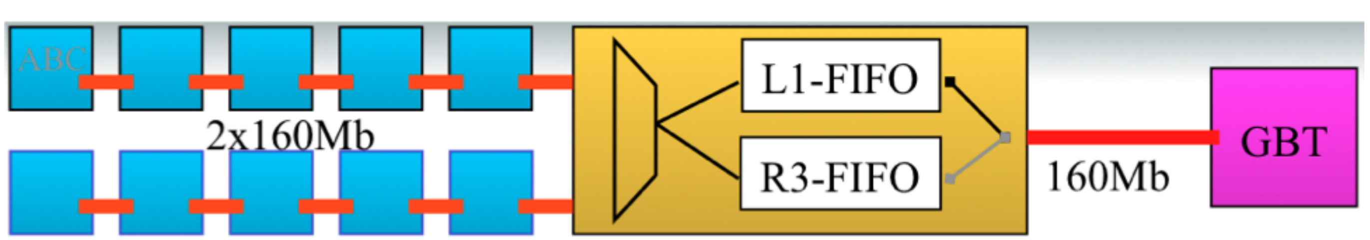
Improved Tracker

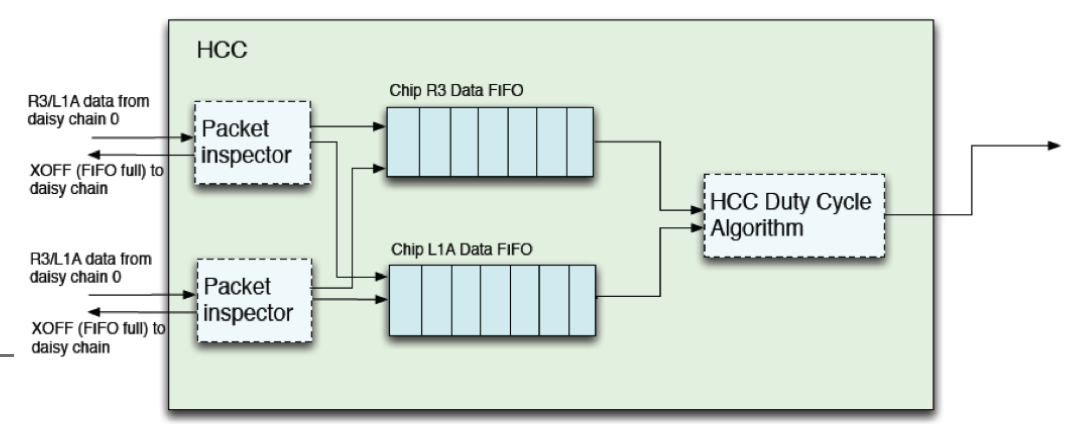
L (fb^{-1})	No. of B_s^0	No. of B^0	$\delta\mathcal{B}/\mathcal{B}(B_s{}^0 \to \mu^+\mu^-)$	$\delta\mathcal{B}/\mathcal{B}(B^0 \to \mu^+\mu^-)$	B^0 sign.	$\delta\frac{\mathcal{B}(B^0\to\mu^+\mu^-)}{\mathcal{B}(B_s^0\to\mu^+\mu^-)}$
20	16.5	2.0	35%	>100%	0.0–1.5 σ	>100%
100	144	18	15%	66%	0.5–2.4 σ	71%
300	433	54	12%	45%	1.3–3.3 σ	47%
3000	2096	256	12%	18%	5.4–7.6 σ	21%

ATLAS L0 and Regional Readout Requests (R3) implementations



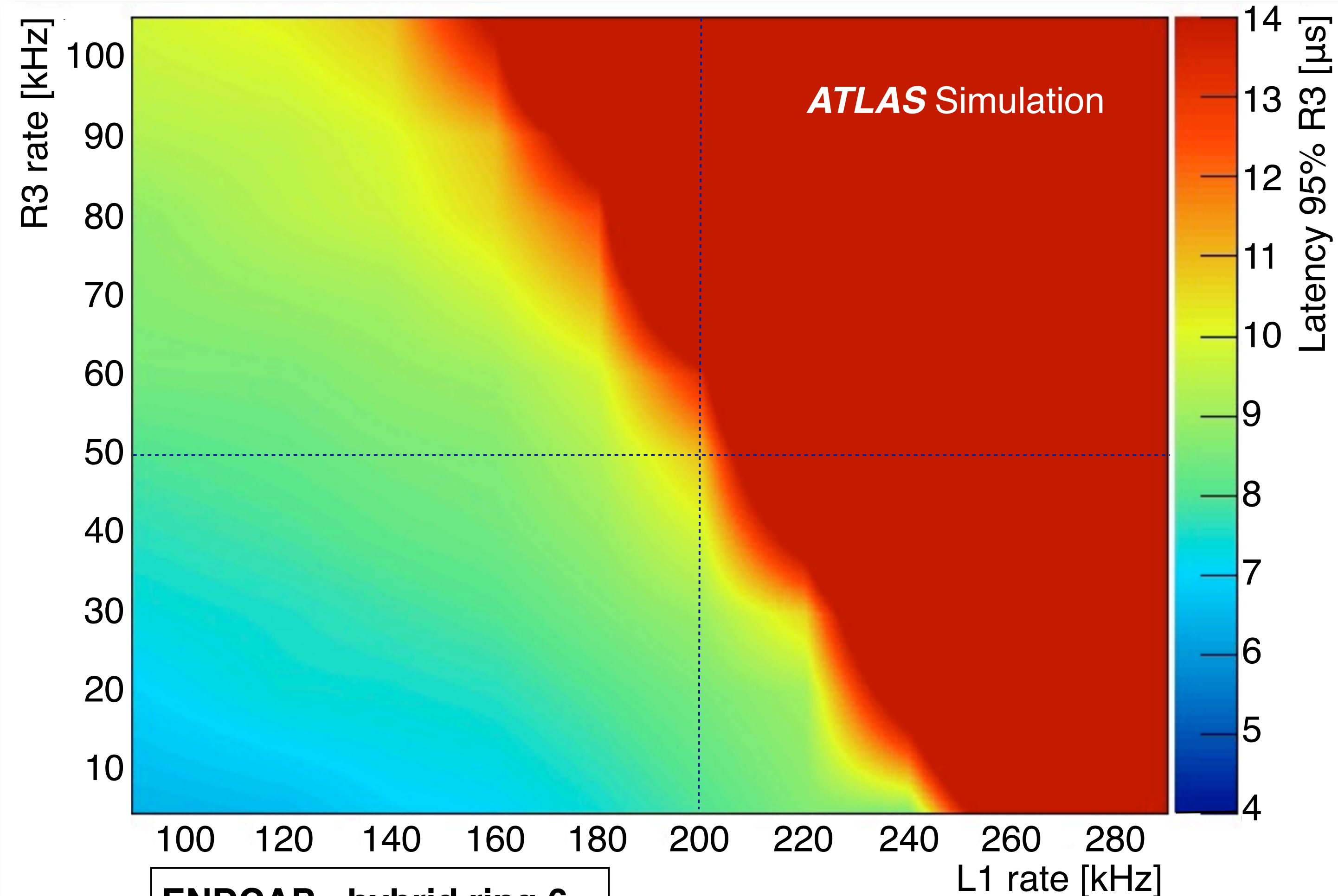
- Trigger data in < 5μs
  - L0 Trigger accept rate 500 kHz
    - On a L0 accept, copy data from primary to secondary buffer
    - Identify "region of interest" (1-10% of the detector on each L0 accept)
    - Generate a "Regional Regional Request" (R3)
      - Reading only ~10% of the Tracker data, the total bandwidth is only 50% more with the Track Trigger than without.
    - To reduce the latency, a prioritization scheme is envisaged, by using a dedicated R3 buffer



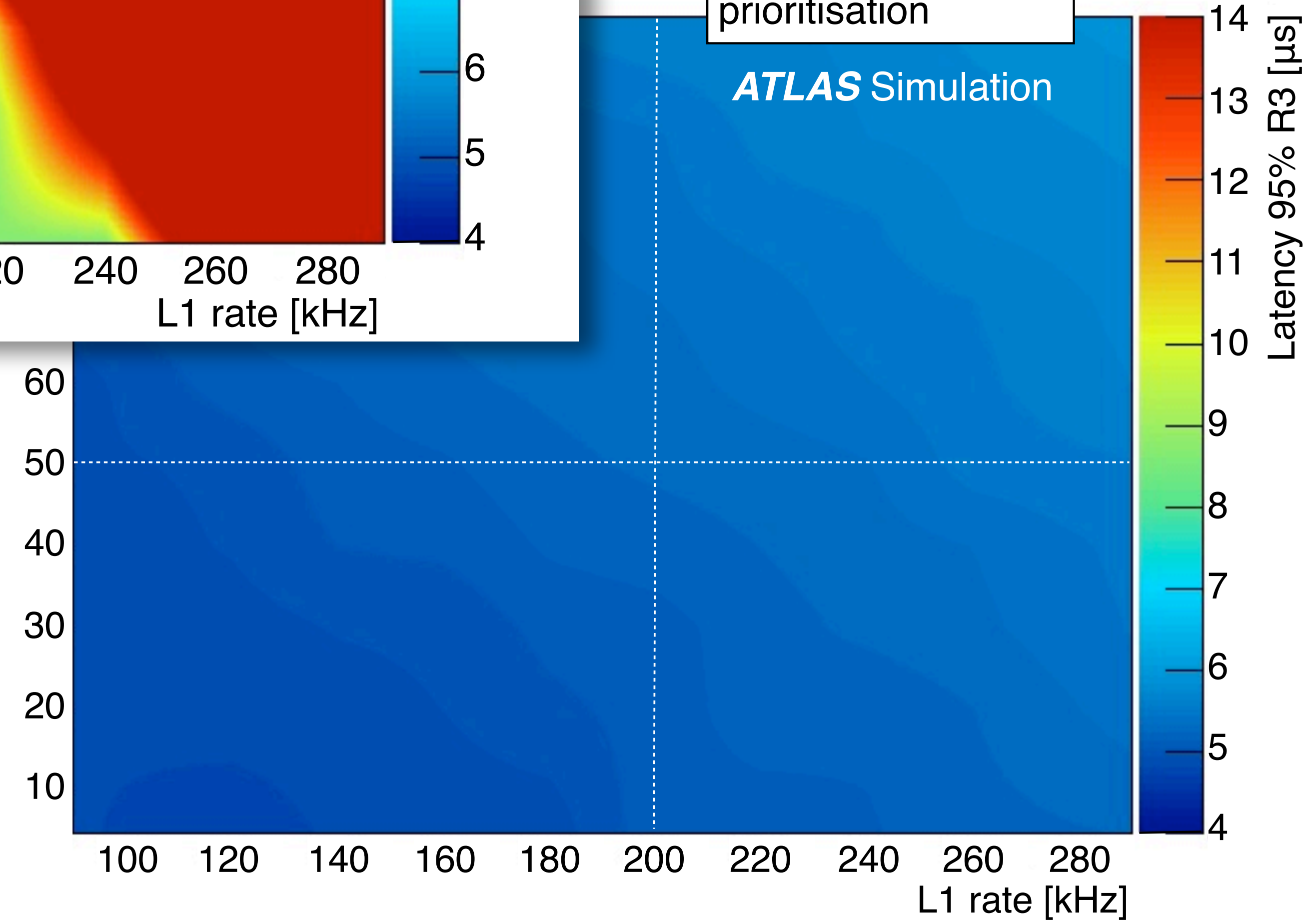


Simulation results - ATLAS

Latency maps



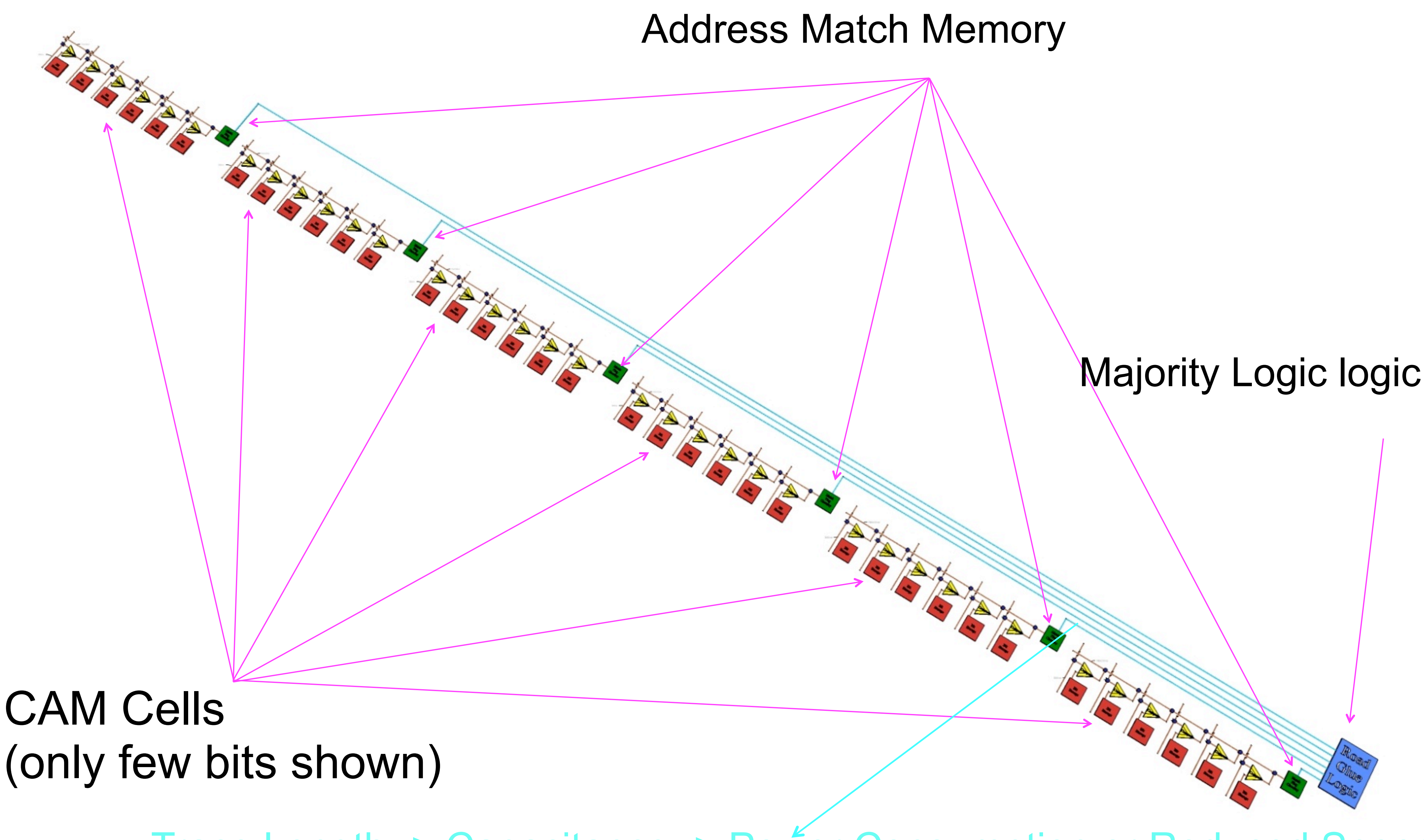
ENDCAP - hybrid ring 6
including R3 HCC
prioritisation



BARREL - layer 0
including R3 HCC
prioritisation

- Barrel acceptable latency over the full phase space when using prioritisation on the HCC
- Endcap hybrids run 4, 5 and 6 have an issue due to limited HCC bandwidth and chip multiplicity

Anatomy of a PRAM
(Pattern Recognition Associative Memory)



Trace Length -> Capacitance -> Power Consumption or Reduced Speed

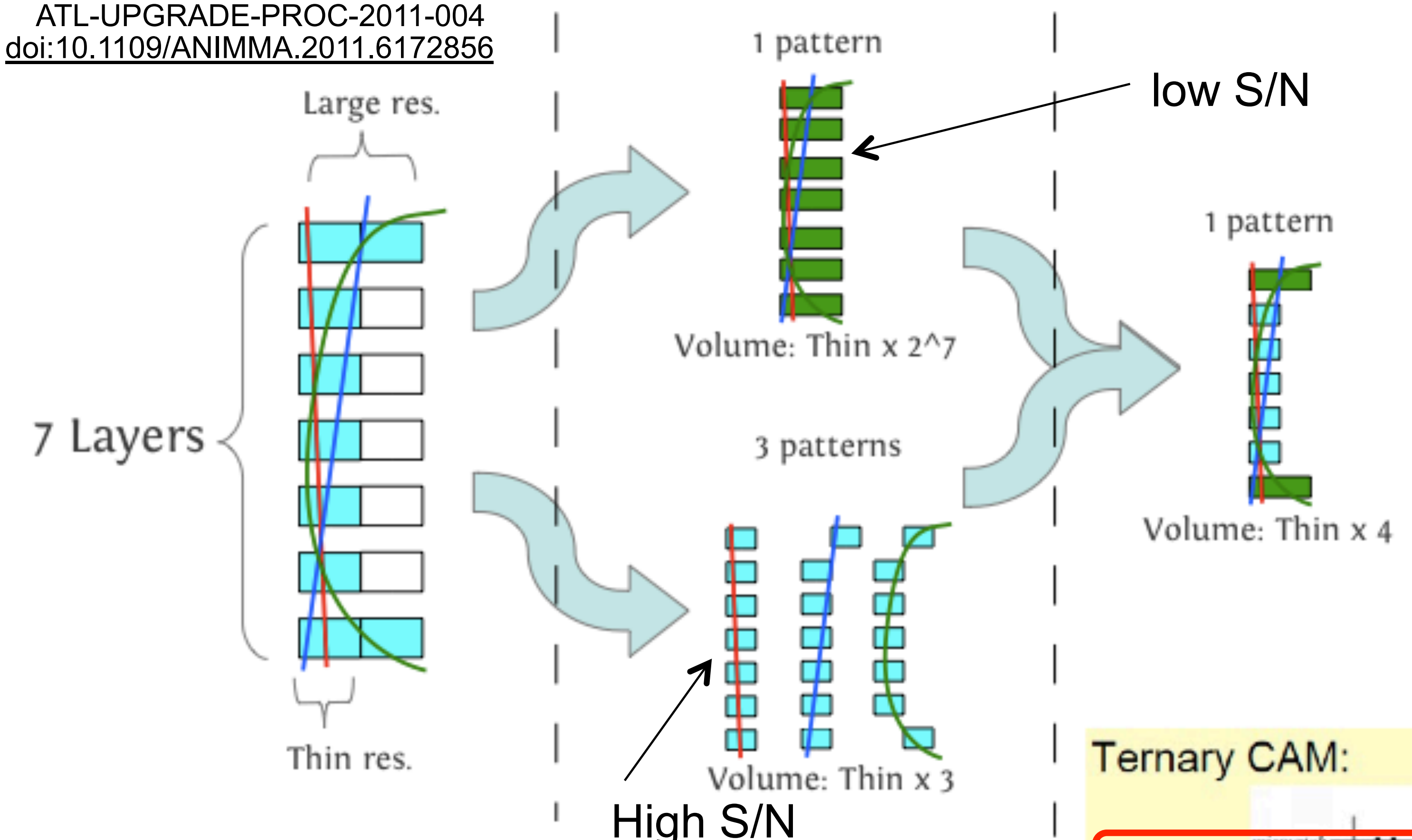
More detector layers, or more bits involved, design more spread out in 2D

→ less pattern density, higher power consumption …

AMCHIP04: VARIABLE RESOLUTION

A new "Variable Resolution Associative Memory" for High Energy Physics
ATL-UPGRADE-PROC-2011-004
doi:10.1109/ANIMMA.2011.6172856

Fixed resolution | Variable resolution

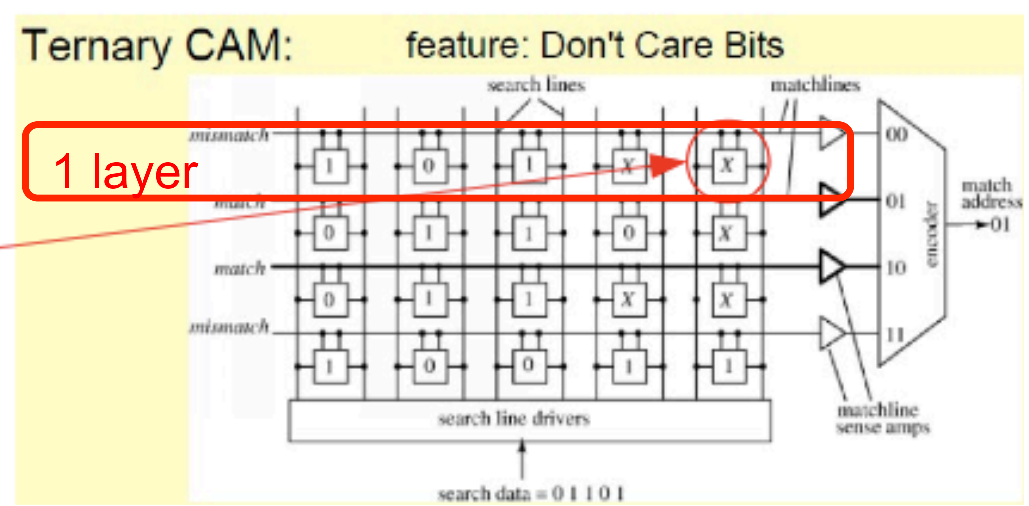


Good rejection and occupy only one pattern location.

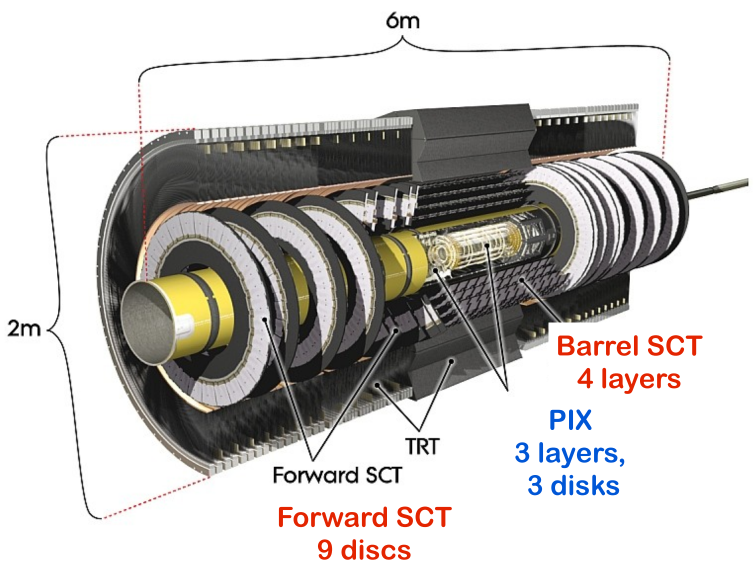
Per-pattern choice of optimal resolution.

We can use **don't care** on the least significant bit when we want to match the **pattern layer @ Large resolution** or use all the bits to match it **@ Thin resolution**

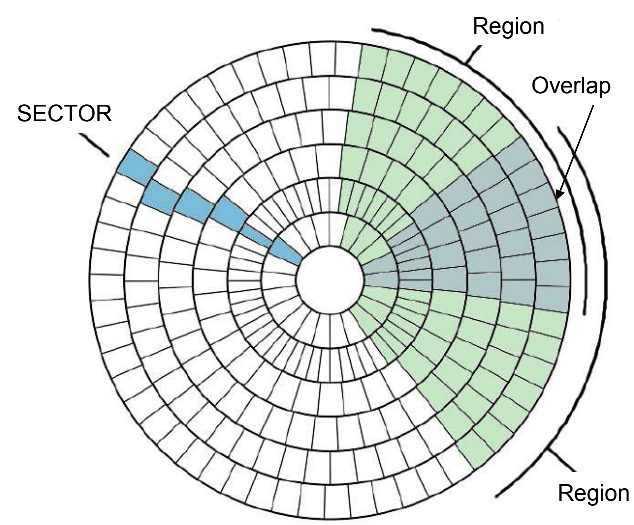
Coincidence window is programmable layer by layer and pattern by pattern



ATLAS FTK



- To deal with data flow designed as highly parallel system
  - 8 ‘core crate’ with own pattern recognition and track fitter
  - Detector subdivided in 64 trigger tower



- PIX (3 layers) & SCT (4 double layers)
- Fit posses combinatorics problem, executed in two sequential steps:
  - Use 8 layer for patter recognition and 8 layer fit
  - Refit track found using all 11 layer