ARIES Workshop on Energy Efficient RF
Ångström Laboratory, Uppsala, 18-20 June 2019

Plenary discussion: Future of Solid State

Jörn Jacob, ESRF (chair)

Radio Frequency (RF) Solid State Amplifiers (SSA) for high power applications have been pioneered and operated for many years with an extremely high reliability at SOLEIL (352 MHz SSA). After a first transfer of technology to the industry (e.g. from SOLEIL to ELTA, for the ESRF), or by combining existing products to obtain larger power (e.g. Bruker/SigmaPhi 1.3 GHz SSA for SC-Linacs), the technology is now proposed by an increasing number of industrial suppliers (e.g. THALES&GERAC pulsed SSAs at 200 MHz for CERN/SPS, IBA SSA at 176 MHz for MYRRHA, Rohde & Schwarz for MAX IV and SOLARIS, CRYOELECTRA for BESSY, and many others…). Despite the successful implementation of SSA at many accelerator labs, for each new accelerator project the choice between solid state technology and vacuum tubes must be re-addressed.

In the context of this ARIES workshop, the achievable supply to RF power conversion efficiency of SSA technology was addressed in several dedicated talks.

V. Carrubba (Ericsson AB) reported on the Doherty configuration with several transistor stages that allows operating an amplifier module at high efficiency over a large dynamical range (for instance 12 dB range with a 3 way Doherty). This is a standard configuration in telecommunication systems. Also GaN technology can potentially provide 10 % more efficiency than still mostly used Si-based LDMOS FET (80 to 85 % DC to RF could still be achieved at 2 GHz with GaN technology).

Envelope Tracking (ET) is an alternative to Doherty and consists in adjusting the DC supply voltage to the power demand, therefore always operating the SSA close to maximum achievable efficiency. In digital communication, the input signal strength is then used to modulate the envelope. This principle is also under development at several places for accelerator applications.

At the transistor level the efficiency can be increased by keeping the temporal overlap of large voltage and high transistor current short and thereby minimizing the transistor losses. This is typically the goal with higher classes of transistor operation like E or F, as addressed by Olof Bengtsson (Ferdinand Braun Institut). Transistors are then operated in switched mode and/or harmonic impedances are adjusted such that harmonics help minimizing switching time.

Paul Tasker (Cardiff University) showed that when exploring limits of achievable efficiency, every amplifier stage has to be optimized, starting with the power supply (e.g. direct AC mains to DC supply conversion) and ending with the power combiner. For instance, the increasingly adopted single stage cavity combiner, first proposed by the ESRF, can improve the combining efficiency as compared to a multi stage coaxial combiner, and it allows easily tailoring the number of active amplifier modules to the required output power.

The following points were proposed at the plenary discussion on Solid State Power amplifiers:

1) *Since pioneering at SOLEIL for accelerator applications:*
   - *SSA increasingly proposed by industrial suppliers*

- *Increasing experience with high power applications (SPS hard time -> learning effect)*
- *Frequency range: up to ≈1 GHz in LDMOS technology*
- *Further into GHz range with GaN technology*

2) *Which argument prevails for different applications, power ranges, e.g. Light sources vs High energy physics machines or Small labs vs. Large facilities in terms of:*

   - *Procurement costs / Possession costs (SOLEIL, ESRF experience)*
   - *Is SSA technology plug and play?*
   - *Ease of Maintenance and operation (no HV, no X-ray shielding)*
   - *Reliability: modularity, redundancy*
   - *Foot print, Space requirements*
   - *Achievable Efficiency*
   - *Pulsed vs CW operation (see e.g. pulsed S-band 40 MW klystrons not to be replaced with SSA)*
   - *Is Solid state in general still reasonable for 10…100 MW applications (with several 10^4 to 10^5 RF modules)?*

3) *Perspectives in terms of*

   - *Efficiency (Push pull AB +Balun, Single ended, Doherty, Class E, F, G, S, requested RF power reserve by LLRF …)*
   - *R&D for solid state devices -> LDMOS-> GaN, or higher drain voltage, lower C_{ds}*
   - *Which professional / manufacturer would work for accelerator community (small market as compared to telecom)?*
   - *Redundancy: Drive chain, amplifier stages, Modular Power supplies*
   - *Direct AC/DC conversion?*
   - *Fine tuning capability vs design for mass production (efficiency optimization vs fabrication cost)*
   - *Space: coaxial combiner tree vs cavity combiners*
   - *Maximum power per RF module*
   - *Reliability: early fragile -> today rugged transistors*
   - *Lifetime? Related to transistors' temperature, strong demand for the cooling system*
   - *Durability / Obsolescence management / Industry commitment*

4) *Operation parameters*

   - *Power margin vs efficiency optimization*
   - *Dynamic Efficiency optimization by Drain voltage modulation, Envelope tracking (ET), Doherty, …*
   - *Cavity combiner allows tailoring SSA to maximum power requirement*
   - *Protection / sophistication versus simplicity/reliability?*

PLENARY DISCUSSION:

The plenary discussion was driven by the question: for which kind of high power accelerator application does solid state technology constitute a workable alternative to vacuum tubes? The three experts from outside the accelerator community (V. Carrubba, O. Bengtsson, P. Tasker) were asked to appreciate how far the techniques in development for modern telecommunication can be applied to high power RF systems for accelerators. The discussion focused on the following main points:

- Efficiency

  While Envelope tracking is increasingly implemented in accelerator applications, it appears that so far they mainly use LDMOS class AB amplifiers, mostly in push-pull. At FREIA a 1 kW / 100 MHz class E amplifier has been built with an efficiency reaching 87 %. The experts pointed out that class F configuration with dedicated idle harmonic circuits should be feasible also for accelerator applications. However, often the high power MOSFET devices are built of many parallel transistors within a common case, including matching circuits. Class F could possibly be implemented more effectively if the harmonics circuits were integrated in the device. This lead to the next question.

- Tailored transistors for accelerator applications?

  For their pioneering work, SOLEIL had to use custom transistors, which was very successful, but still with 2 % of transistors failing per year. Later on, mass-produced transistors with optimized fabrication processes came on the market, which turned out to be much more rugged and nearly never fail. While it is certainly worth developing components dedicated to the huge telecommunication market, it is unrealistic to believe that large semi-conductor suppliers would develop tailored transistors for accelerator applications. Even for 100 MW projects like FCC-ee the number of needed transistors would remain small as compared to telecommunication applications.

  O. Bengtsson pointed out that the Ferdinand Braun institute would be a candidate for developing custom devices for accelerators, for instance to push the efficiency. GaN technology exhibiting fast switching capabilities and breakdown voltages of typically 600 V are being evaluated for switched mode amplifiers. In collaboration with the Ferdinand Braun Institute FREIA is currently building a load pull measurement system to evaluate new transistors.

  For each particular project one must evaluate the gain in performance with a custom transistor against the risk of reduced reliability and possible earlier obsolescence and compare it to the use of mass-produced devices optimized for telecommunication applications.

- Footprint

  It is generally admitted that the footprint of a MW SSA system is considerably larger than the space needed for a comparable MW klystron transmitter, even though a fair comparison is not obvious. However, for the 4 MW 200 MHz upgrade of the CERN/SPS RF system, for instance, a building had been constructed to provide space for conventional tetrode amplifiers, which will finally house 4 MW of SSA amplifiers. Here the compactness of SSA cavity combiners and the relatively small unit power of tetrodes lead to quite similar space requirements.

  The question whether the footprint could possibly kill the SSA solution as compared to dedicated high power klystrons for extremely high power applications like FCC was not clearly answered.

  So, no general statement can be made and a case by case evaluation of the foot print and its impact on the decision for or against SSA technology is required.

- How much diagnostics?

  One of the greatest fears when implementing high power SSA is uncontrolled, massive deterioration of transistors, although this was never reported for existing SSAs in the last decades. This fear drives a natural tendency to implement many diagnostics and protections in order to detect and understand any malfunctioning before it harms the system. For SSA with many hundred amplifier modules, sophisticated diagnostics drive costs and may reduce the overall reliability of the system. Moreover, producing many data makes only sense if these data are efficiently monitored and processed and if most of the protections act on individual modules and not on the amplifier as a whole.

  A discussion pro and against many diagnostics showed that a number of diagnostics are often requested by the operators to gain confidence and understand the behavior of their SSA systems. However, a reduced number of diagnostics is generally felt sufficient to still well monitor the operation of a system.

At least must a malfunctioning amplifier module be identified such that it can be replaced at time. Note that per design, thanks to their modularity and with a reasonable power overhead, a SSA should never trip even with a few missing or defective RF power modules.

CONCLUSION:

Several ways have been identified that could push SSA efficiencies for accelerator application towards the 80 % level up to the GHz range. However, as was stated during the discussion on efficient vacuum tubes, it is only by really implementing such solutions at a larger scale on a real accelerator project that one could validate such approaches.

The compromise between pushing efficiency to maximum or privileging reliability and power margin must be defined case by case.