Upgrading the ATLAS detector; why do we do it and how is it done?

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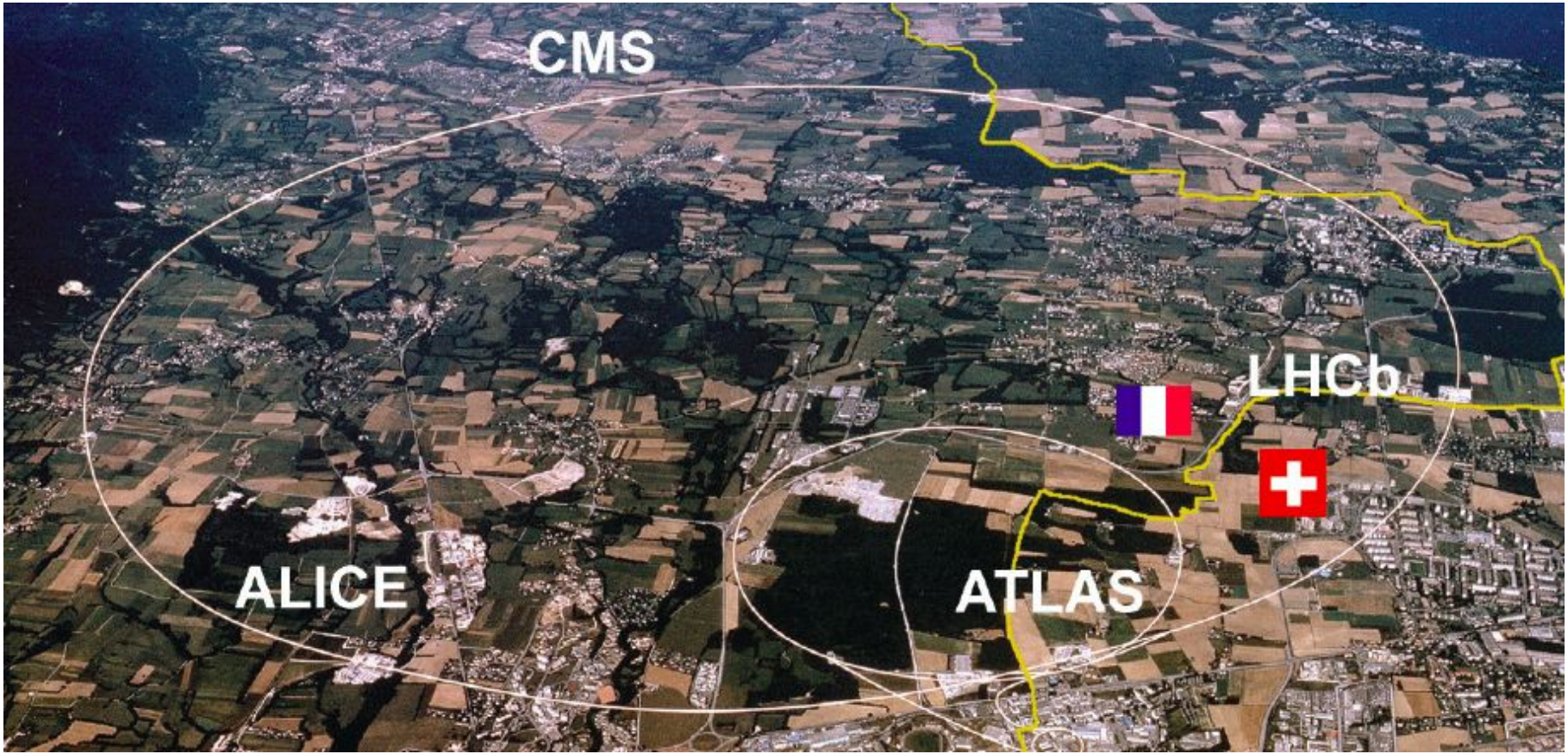
ATLAS
SCANDINAVIA

UPPSALA
UNIVERSITET

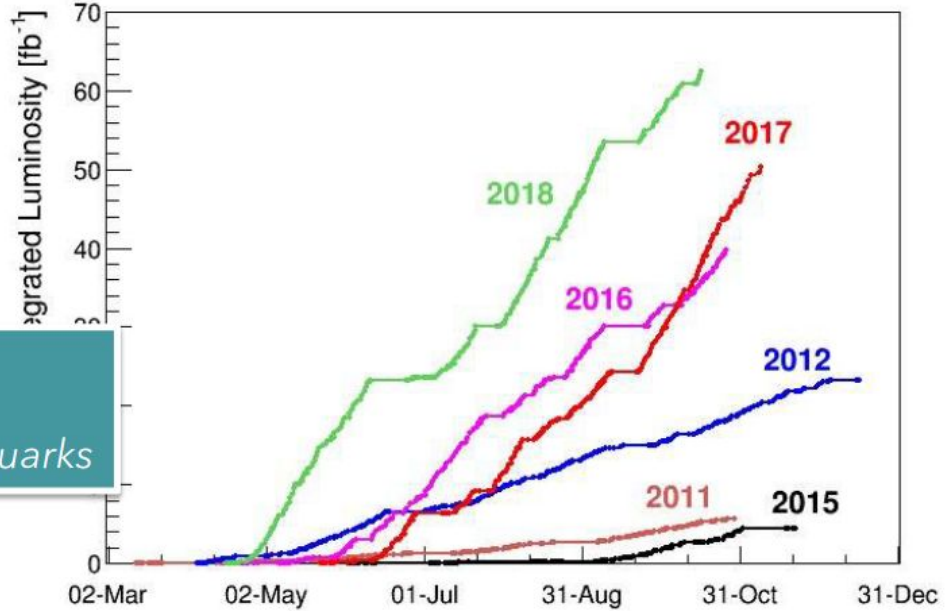
- HL-LHC
  (High Luminosity LHC)
- How does these changes effect ATLAS?
- ITK
  (Inner Tracker)
- HTT
  (Hardware Track Trigger)

Large Hadron Collider (LHC)



LHC - A Huge Success

- Run-1 (2010-2012)
  - **~5fb^{-1}** of pp collisions at 7TeV and **~20fb^{-1}** at 8TeV
- Run-2 (2015-2018)
  - **~150fb^{-1}** of pp collisions at 13TeV



Roughly, per big experiment
- *8M of Higgs bosons*
- *178M of events with top quarks*

- Higgs boson discovered in 2012
- Nothing new since then - all measurement compatible with Standard Model

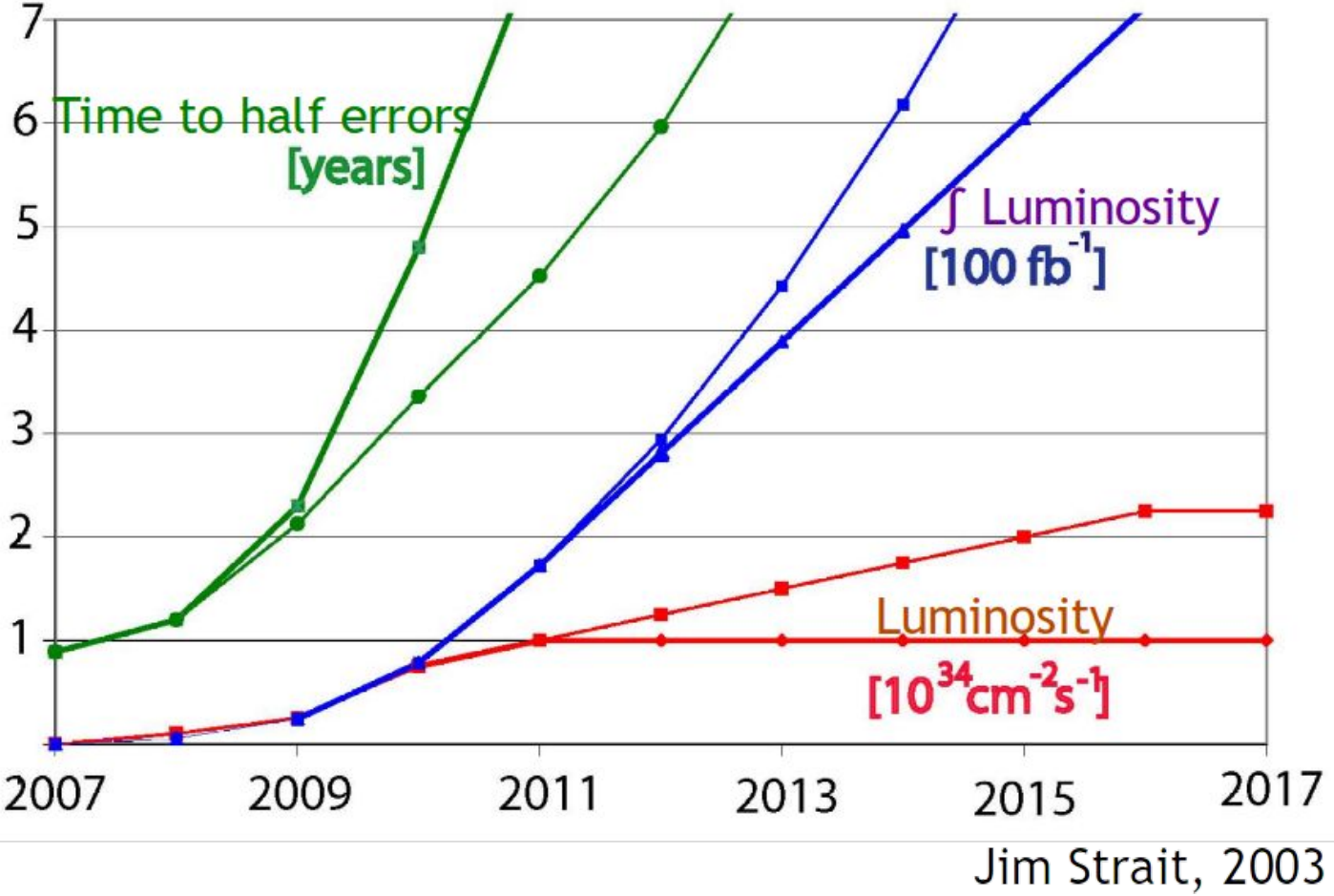
So, are we done?

Outstanding problems in Elementary Particle Physics

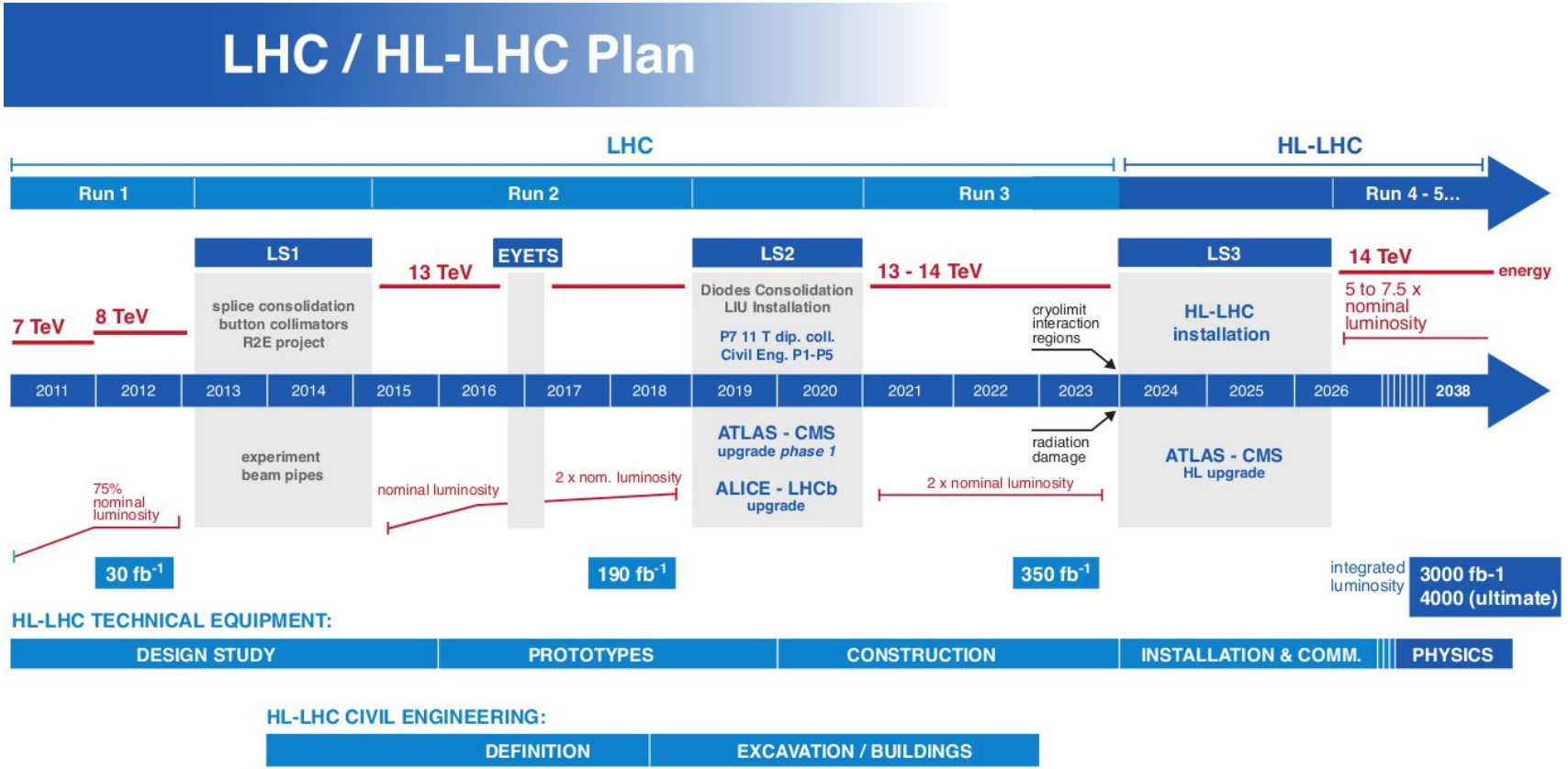
- Gravity?
- Neutrino masses?
- Why three generations of fermions?
- Baryon asymmetry?
- Dark Matter?
- Dark energy?
- And more...

Do we just keep running the current LHC?

No:
Diminishing returns on information gain!



Need to upgrade!



HL-LHC upgrade

Parameter	LHC Run-1	LHC Run-2 & 3	HL-LHC
Beam energy [TeV]	0.45–4	6.5–7	7
Peak inst. luminosity [$cm^{-2} s^{-1}$]	$0.8 \cdot 10^{34}$	$(0.7–2) \cdot 10^{34}$	$5 \cdot 10^{34}$ (levelled)
Bunch distance [ns]	50	25	25
Max. number of bunches	1380	2028~2748	2748
β^* [cm]	60	40	15
ε_n [μm]	2.3	2.5–3.5 (2.3 with BCMS)	2.5
Max. num. protons per bunch	$1.7 \cdot 10^{11}$	$1.2 \cdot 10^{11}$	$2.2 \cdot 10^{11}$
Average pileup ⟨μ⟩	21	21~50	140
Integrated luminosity [fb^-1]	~26	~350	3-4000

How does HL-LHC effect ATLAS?

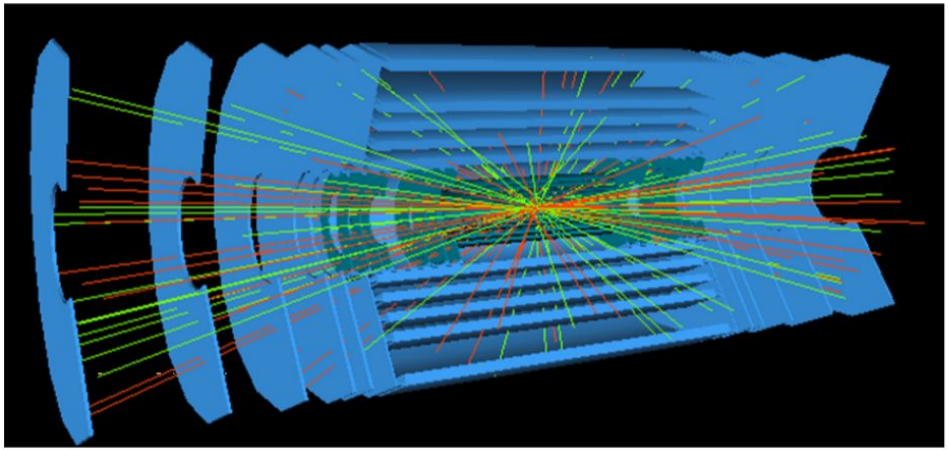
- **Radiation Damage**
  Current Inner Detector(ID) will be worn out by end of Run 3.
  Not feasible to replace it with a carbon copy, much more radiation hard design require for HL-LHC

- **Pile up: Detector Occupancy**
  Current ID designed for pile-up <μ> ~ 50 - HL-LHC will have <μ> ~ 140-200 - **TRT will be <u>blinded!</u>**
  Additional simultaneous events -> added difficulty in differentiating neighbouring tracks.
  Need increased spatial granularity to retain efficiency

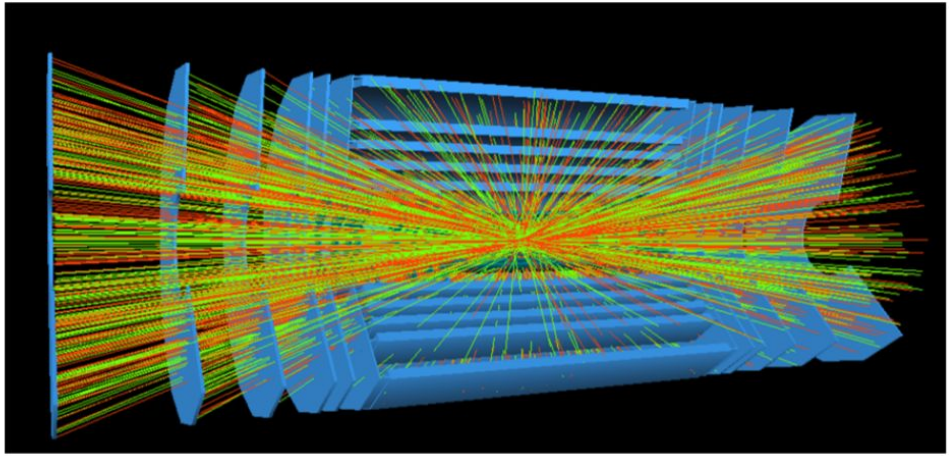
- **Pile up: Bandwidth Saturation**
  Current read-out electronics lacks bandwidth for HL-LHC conditions -> loss of data

- **TDAQ and Trigger**
  Increasing collision rate is a moot point without also improving the triggering scheme. Lower thresholds and more effective online reconstruction is required to benefit - pile-up is the enemy!

Difference in pile-up



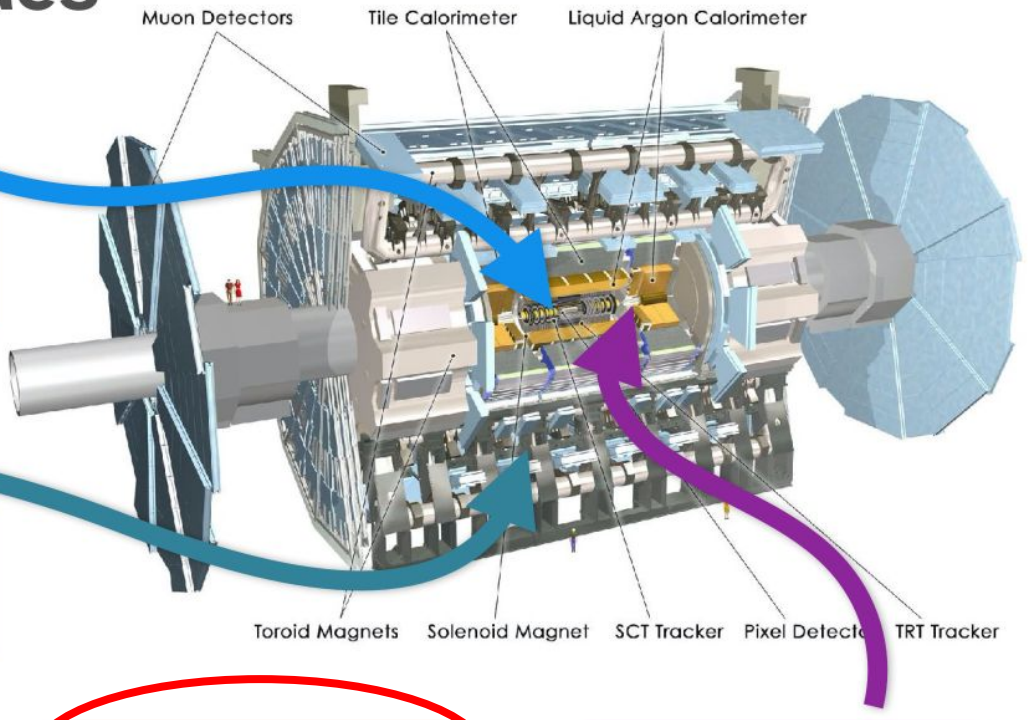
μ = 23



μ = 230

Phase-II Upgrades

ATLAS



Inner Tracker (ITk)

Entirely replace existing tracker
All-silicon, Acceptance for $|\eta|<4$

New Muon Chambers

Chamber replacement in inner barrel

Electronics Upgrades

LAr, Tile, Muon Systems

Trigger/DAQ

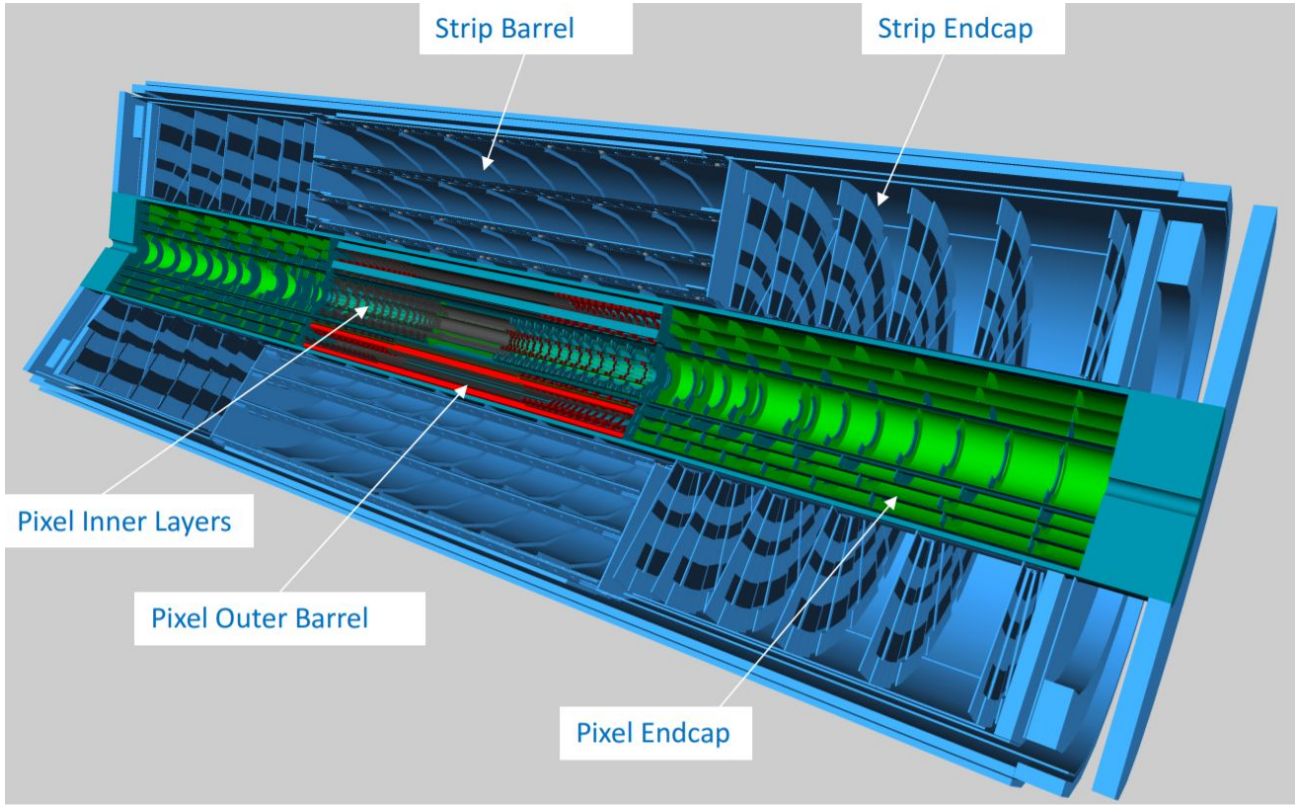
Upgrade to L0-based system at 1 MHz

High Granularity Timing Detector

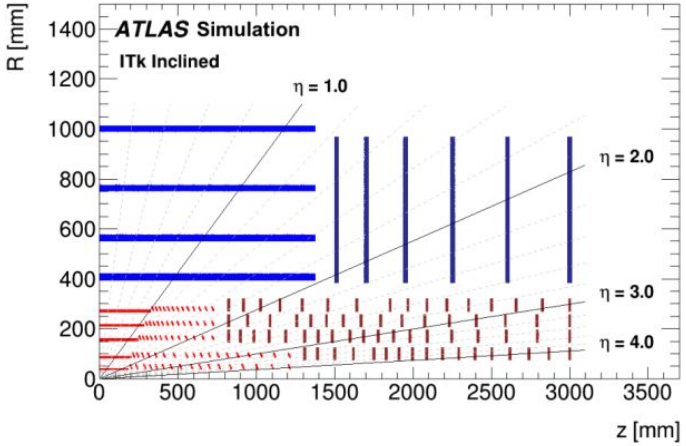
Forward timing coverage from LGADs w/ 30-50 ps resolution for MIPs

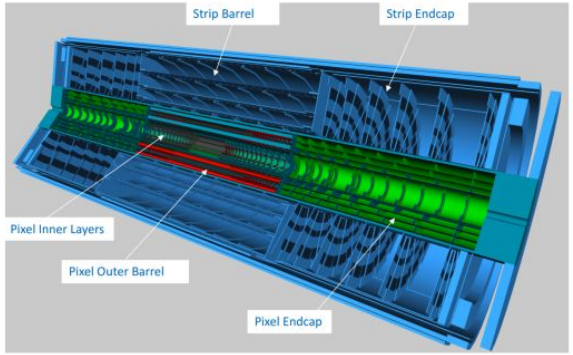
Inner Tracker (ITK)

- All silicon detector to replace current ID and TRT.
- Modular structure consisting of ~20.000 independent detector modules
- ~60 M data channels in total - majority in the pixel layers.
- Hardware cost will be ~300 MCHF

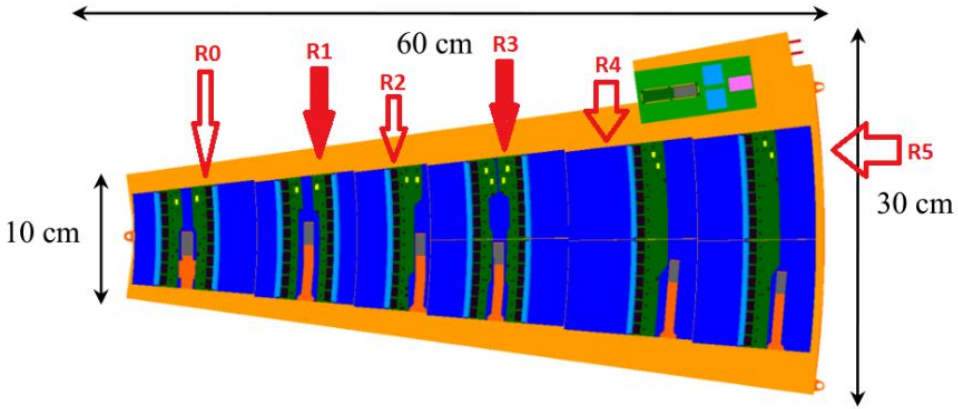


ITK Structure



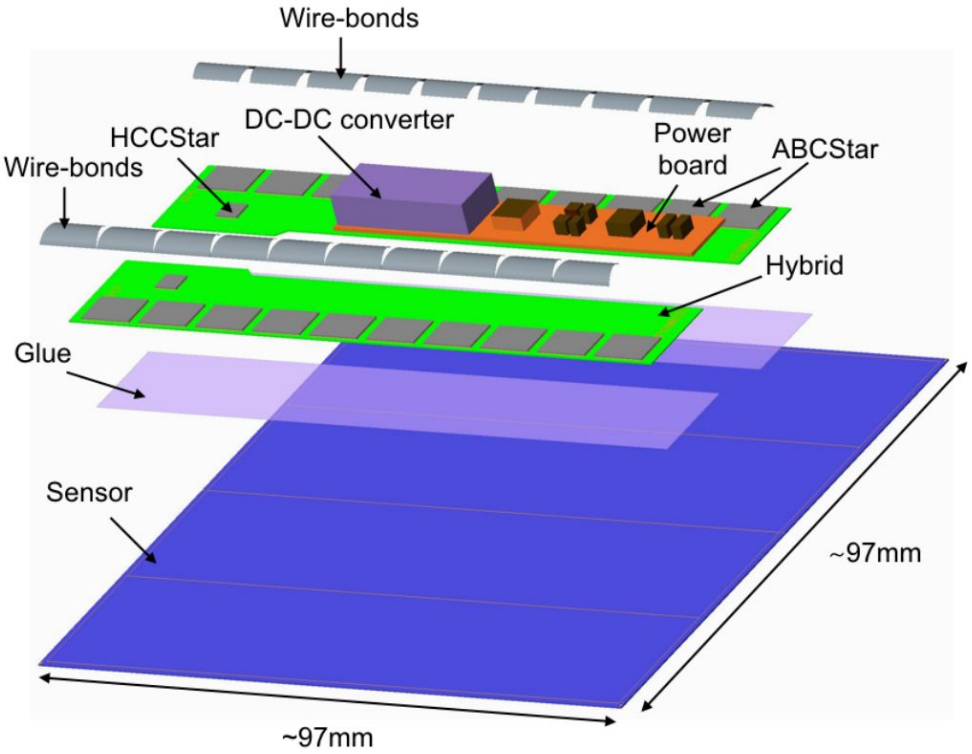


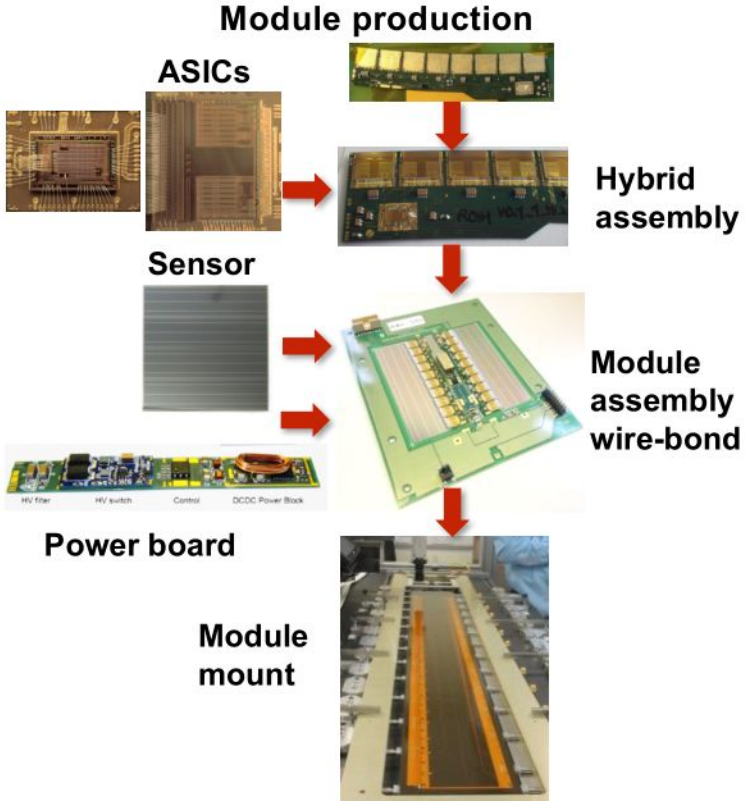
Cross section of ITK, red are pixel modules and blue strips.



Endcap rings made of petals, based on 6 module geometries.
The Scandinavian Cluster will produce ~ 600 modules of types R1 and R3.
Only R0 components available for prototyping.

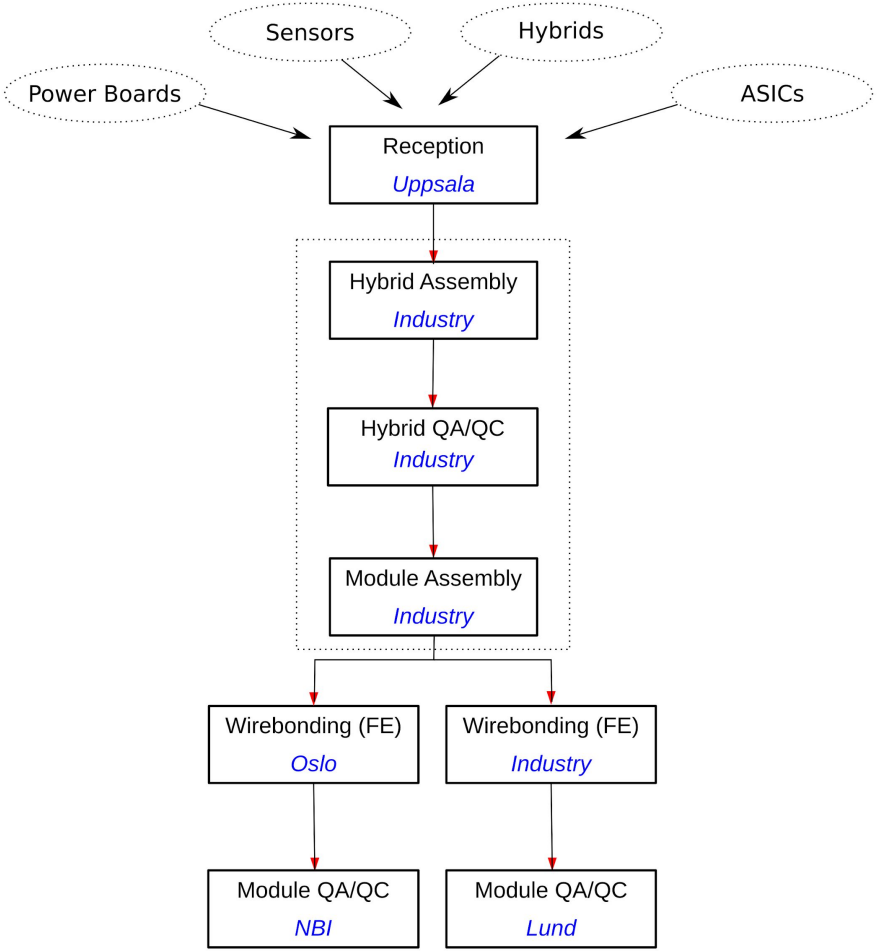
ITK module


Wire-bonds
HCCStar
DC-DC converter
Power board
ABCStar
Wire-bonds
Hybrid
Glue
Sensor
~97mm
~97mm


Module production
ASICs
Hybrid assembly
Sensor
Module assembly wire-bond
Power board
Module mount

Scandinavian ITK Cluster

- Copenhagen, Lund, Oslo and Uppsala have joined forces to accumulate sufficient manpower.
- Will deliver 10% of the endcap strip modules ~666 in total
- Uppsala collaborates with swedish electronics manufacturer NOTE



Examples of projects

1. Developing and maintaining a glue robot for automation of assembly line at industry.

   Control of hardware, calibration of behaviour and development of accessible UI for industry operators

2. 3-D modelling custom tools needed for production line.

3. Electrical testing, convolution of hardware and software debugging.

4. Ion beam analysis of water content in silicon sensors

5. Develop production flow; prove we can produce modules within spec in an **scalable** manner

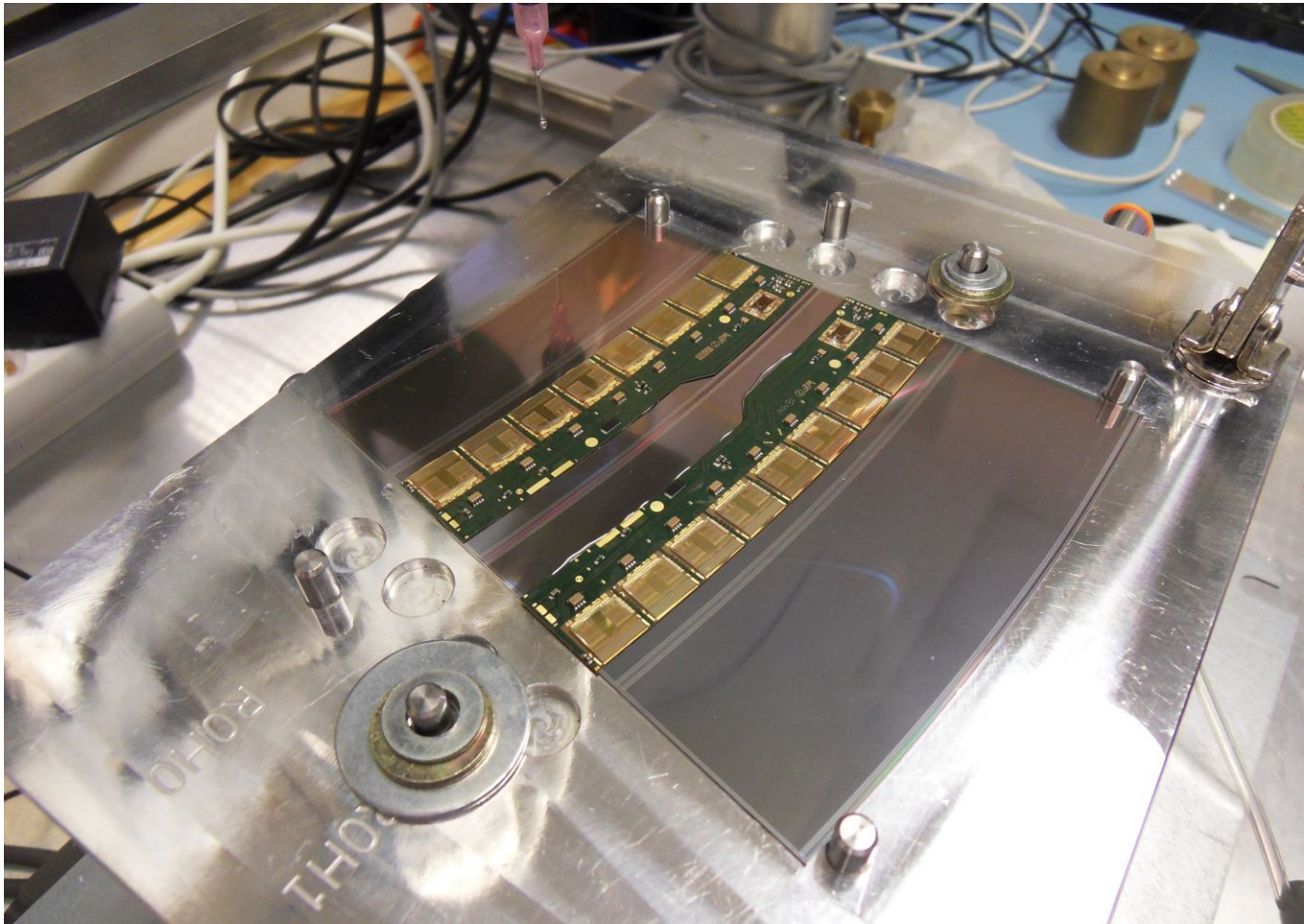
Milestones are dynamical in a production environment. What is relevant to work on evolves over time in unpredictable manner

R0 module:

- 4352 data channels, with 256 per ABC chip.
- Accurate attachment of ASIC's onto the hybrid and hybrid onto the sensor is **critical!**

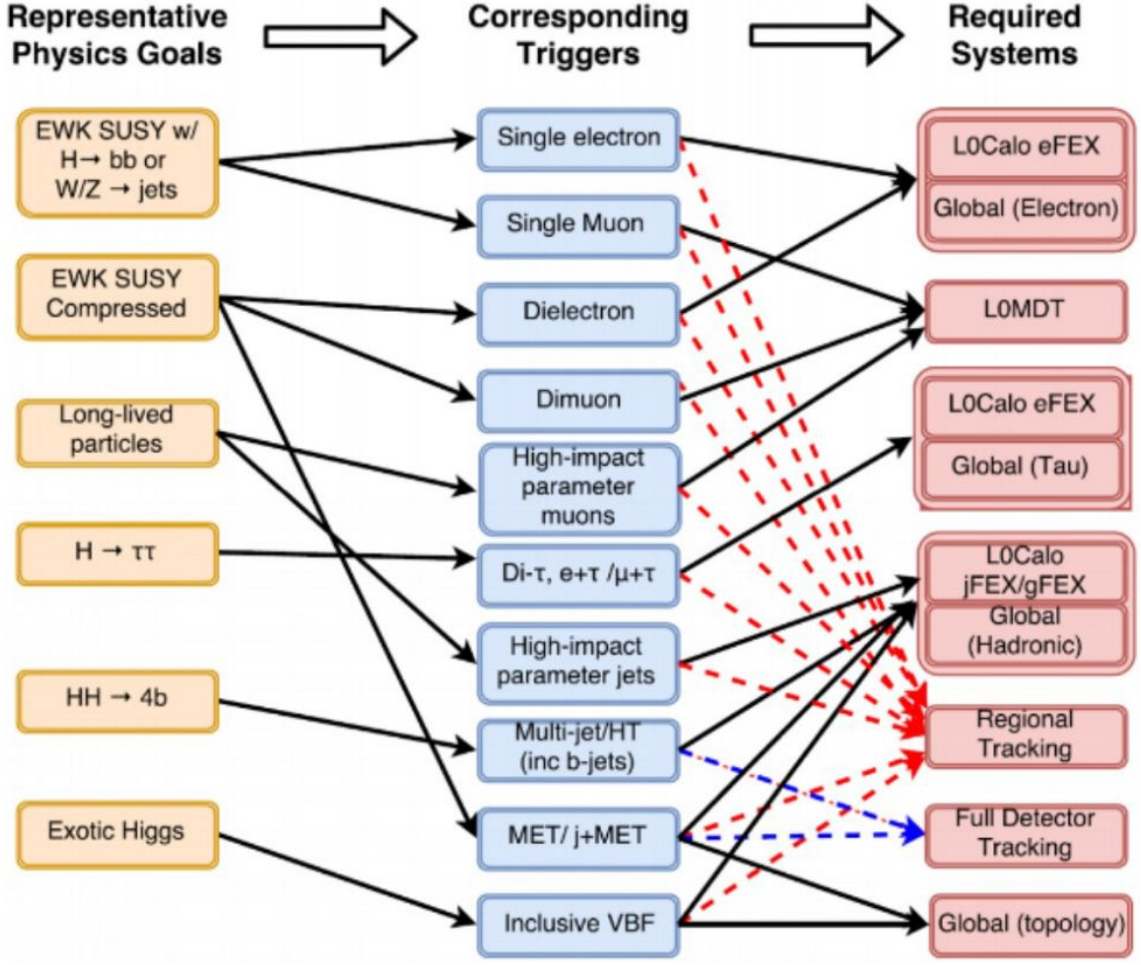
  Failure -> loss of data.

(Powerboard havent been attached on this picture yet)



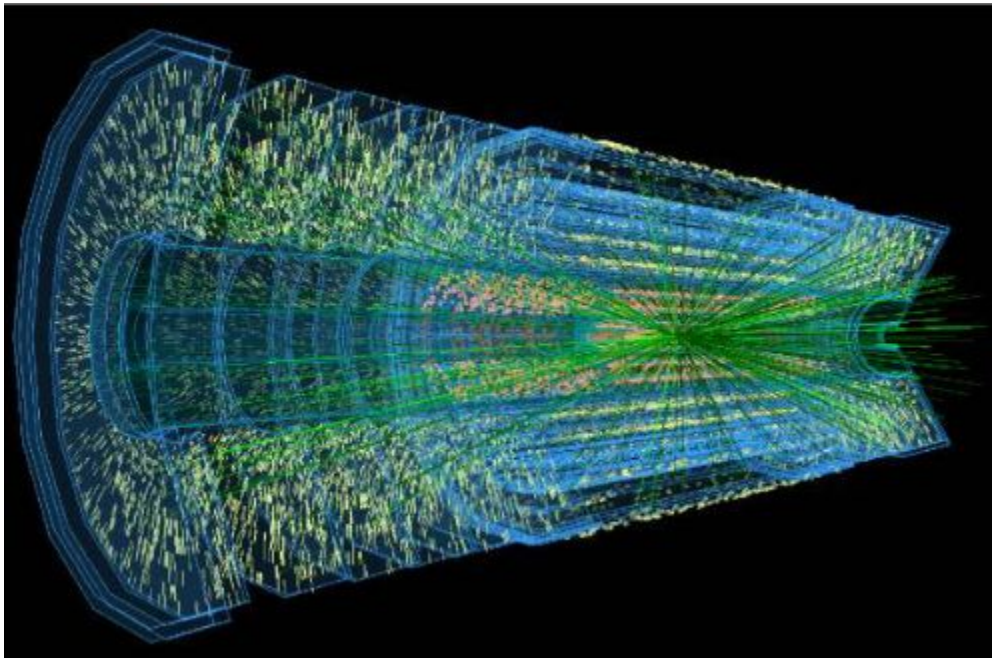
ATLAS trigger menu

- Too much raw data, can't save it all.
- Trigger menu maps interesting physics to detector signatures.
- From 40 MHz collision rate to 10kHz read-out to permanent storage
- Red and blue indicates event types HTT would help identify.



Tracker Triggering

- The increase in pile-up will make reliable and efficient event reconstruction more difficult.
- For charged particles, the tracker can help greatly with this.



- The Hardware Track Trigger (HTT) will combine custom AM ASICs for pattern recognition with FPGA's for track fitting and reconstruction

- This is faster, cheaper, more climate friendly and more scalable than a typical CPU farm (1MHz -> 4MHz)

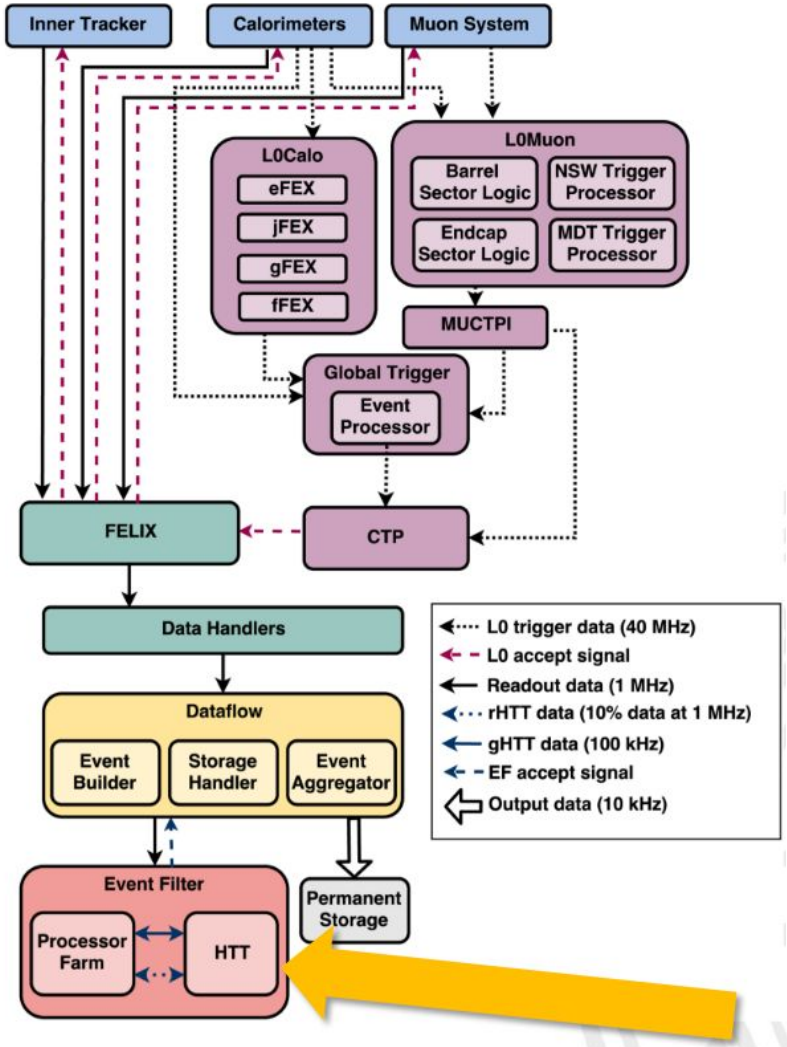
(HTT will be a supplement to the existing CPU farm)

ATLAS Trigger structure:

- Purple block takes trigger data at 40 MHz
- If triggered, Central Trigger Processor (CTP) sends command for full detector read-out at 1MHz

- Temp storage while Event Filter evaluates events

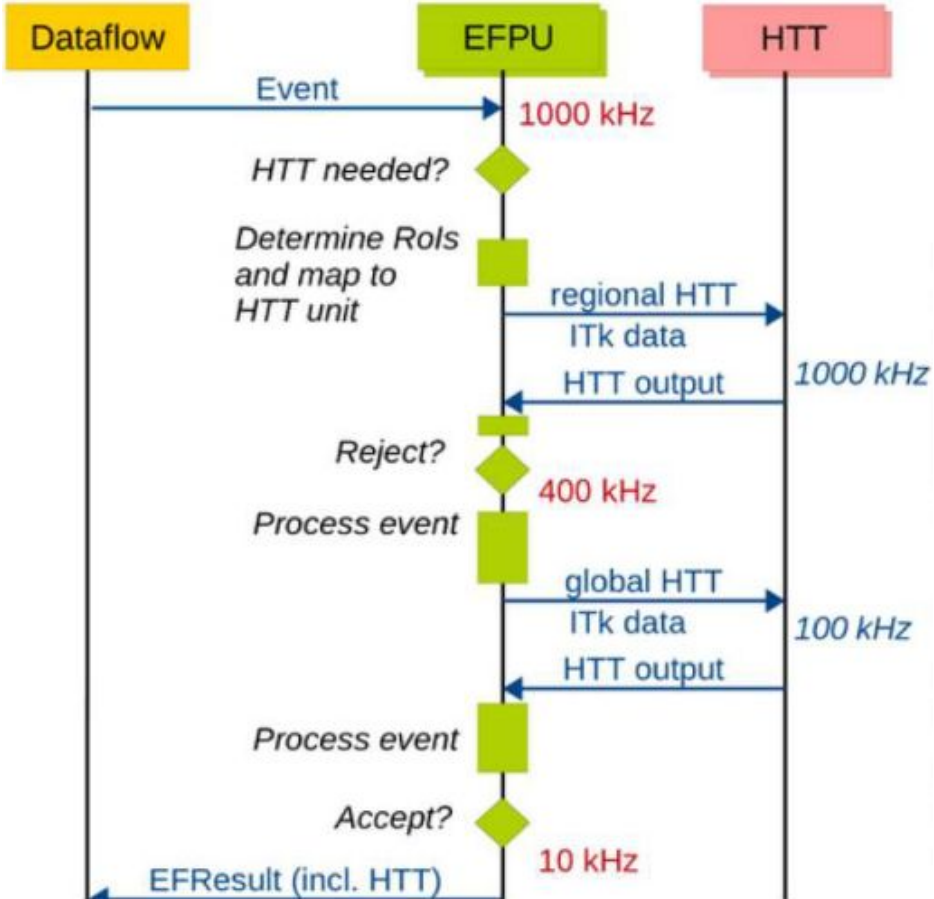
Possible to upgrade to 4 MHz read-out at a later point, for now focus is getting functional 1Mhz system ready on time (cough cough ITK pixel cough cough)



How will HTT be used:

1. Would L0 trigger signature benefit from the trigger data?

2. Can the trigger signature make do with a regional read-out of the tracker, or is the full picture required?
   (eg.single electron vs multi-jet event)



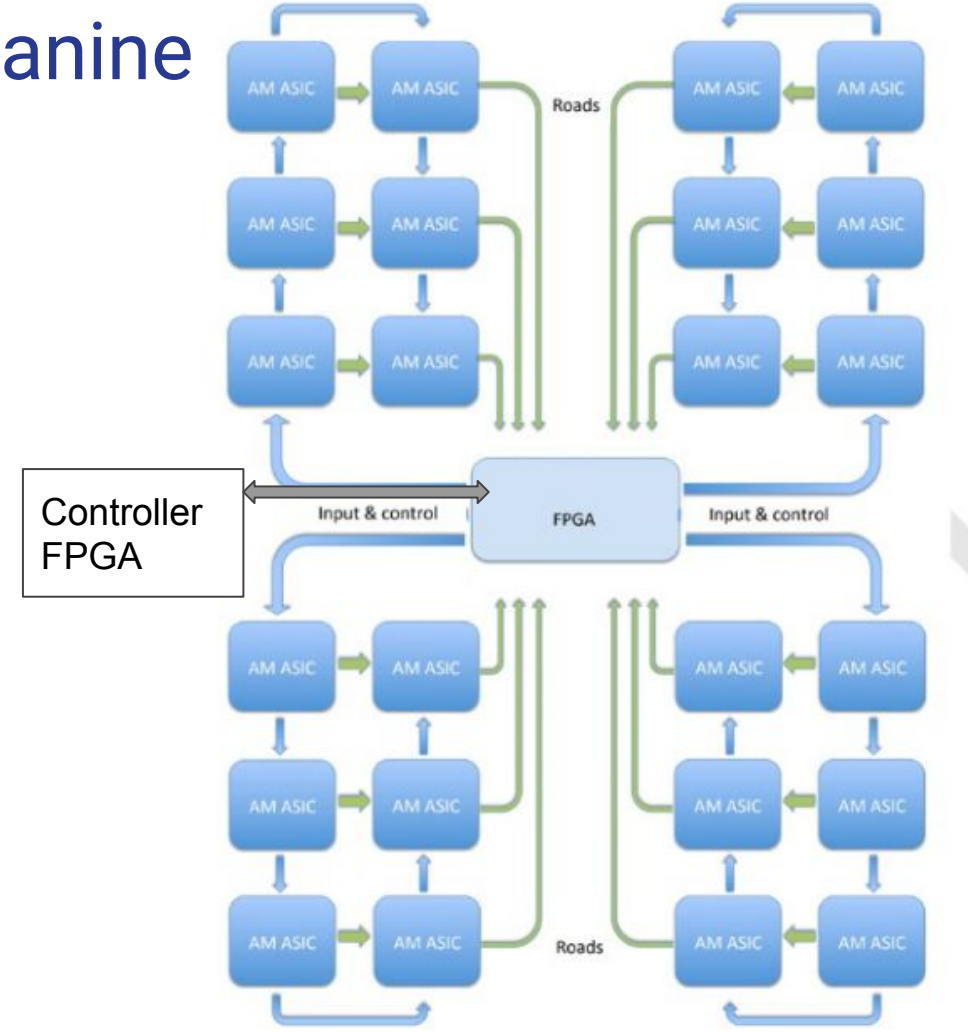
HTT overview

A “motherboard” the Tracking Processor (TP) with two primary blocks:

- Pattern recognition Mezzanine (PRM)
- Track Fitting Mezzanine (TFM)

Pattern recognition Mezzanine (PRM)

1. Associative Memory (AM) asics will store pattern bank of 2.3 M event patterns.
2. Stratix10 FPGA will fit incoming events against these patterns at a rate of 1 GHz.
3. Resulting in an I/O bandwith of 10 Gbps.
4. Max10 FPGA acts as controller, handling powering and monitoring of the stratix10 - so it doesn't burn up..



ATLAS Authorship Qualification task

- Developing monitoring software for the PRM
- In december we will finish construction on a PRM demonstrator board, a proof-of-concept setup. I’m responsible for establishing communication between an ESP232 microcontroller and the MAX10 FPGA, using I2C.
- Building a webserver to display data like device temperature, voltage levels supplied to different components, and any other relevant vitals.
- Will move on to monitoring the communication between the MAX10 and the Stratix10, through IPBus protocol later on.

Thank you for the attention!

Full cleanroom suit and UV goggles during ASIC->hybrid assembly at industry site.